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INDIUM PHOSPHIDE GUNN DEVICES (26-60GHZ).(U)
AUG 79 J D CROWLEY, S B HYDER, B R CAIRNS N00123-77-0459
UNCLASSIFIED NOSC-TD-275 NL

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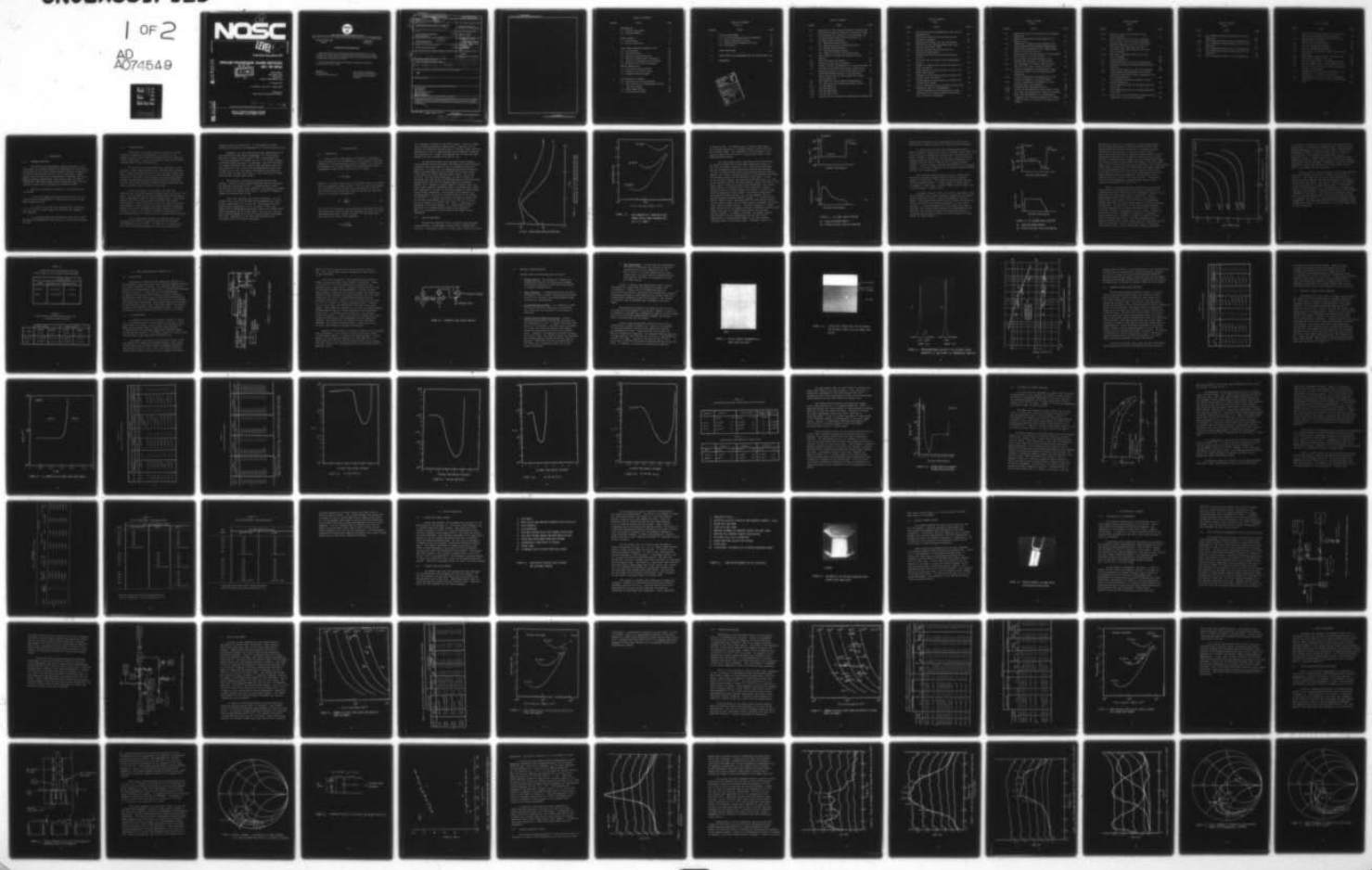

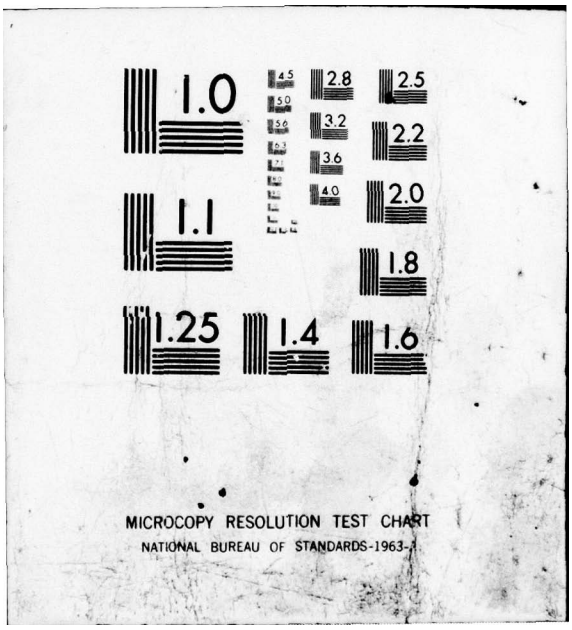
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Technical Document 275

INDIUM PHOSPHIDE GUNN DEVICES (26–60 GHz)

JD Crowley,
SB Hyder, and
BR Cairns
(Varian Associates, Inc)

15 August 1979

Final Report: May 1977 — March 1979

Prepared for
Naval Electronic Systems Command

79 10 02 018

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ADMINISTRATIVE INFORMATION

Work reported herein was conducted at the Corporate Research Laboratory of Varian Associates, Inc, under the direction of F Beringer Fank. This document covers the contract period May 1977 to March 1979. The work was sponsored by the Naval Electronic Systems Command under contract N00123-77-C-0459.

The Navy Project Monitor was D Rubin, Microwave and MM Wave Antennas and Systems Branch (Code 8211), NOSC.

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REPORT DOCUMENTATION PAGE

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1. REPORT NUMBER: NOSC Technical Document 275 (TD-275)
2. GOVT ACCESSION NO.
3. RECIPIENT'S CATALOG NUMBER
4. TITLE *(and Subtitle)*: INDIUM PHOSPHIDE GUNN DEVICES (26-60 GHz).
5. TYPE OF REPORT & PERIOD COVERED: Final-May 1977-March 1979
6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s): JD Crowley, SB Hyder, and BR Cairns (Varian Associates, Inc)
8. CONTRACT OR GRANT NUMBER(s): N00123-77-C-0459
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Naval Ocean Systems Center, San Diego, California 92152
10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 62762N; F54581; XF545810091; 923-EE09P
11. CONTROLLING OFFICE NAME AND ADDRESS: Naval Electronic Systems Command
12. REPORT DATE: 15 August 1979
13. NUMBER OF PAGES: 132
14. MONITORING AGENCY NAME & ADDRESS *(if different from Controlling Office)*: Final rept. 1 May 77-31 Mar 79
15. SECURITY CLASS. *(of this report)*: Unclassified
15a. DECLASSIFICATION/DOWNGRADING SCHEDULE
16. DISTRIBUTION STATEMENT *(of this Report)*: Approved for public release; distribution unlimited

J. D. Crowley, S. B. Hyder B. R. Cairns

17. DISTRIBUTION STATEMENT *(of the abstract entered in Block 20, if different from Report)*
18. SUPPLEMENTARY NOTES
19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

Devices-Fabrication
Gunn amplifiers
Indium phosphide Gunn devices
Microwave amplifiers
Millimeter wave amplifiers

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The program described is directed to the development of InP material and devices for low noise, broad bandwidth amplifier operation in the 26.5 to 40.0 and 40.0 to 60.0 GHz bands. Final objectives are low noise amplifiers covering the 26.5 to 40.0 GHz band and low noise amplifiers with bandwidth greater than 10% covering the 40.0 to 60.0 GHz band.

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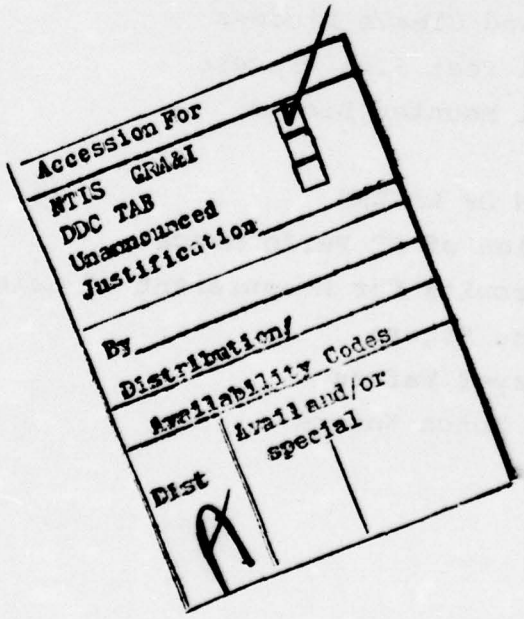

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1. INTRODUCTION

1.1 PROGRAM OBJECTIVES

The research and development program described in this final report is directed towards the development of InP material and devices for low noise, broad bandwidth amplifier operation in the 26.5 to 40.0 GHz and the 40.0 to 60.0 GHz bands. These efforts were initiated by the Semiconductor Microwave R&D Group, Central Research Laboratories, Varian Associates, Palo Alto, California. This final report covers the period from 1 May 1977 through 31 March 1979 on Contract No. N00123-77-C-0459.

The final performance objectives of this program were as follows:

1. Low noise amplifiers covering the full 26.5 to 40.0 GHz band with the bandwidths of 7 GHz, gains of 20 $\pm$ 2 dB and noise figures of 8 dB.

2. A 26.5 to 40.0 GHz full band amplifier with a gain of 20 $\pm$ 2 dB and a noise figure of 8 dB using the staggered gain approach.

3. Low noise amplifiers covering the full 40.0 to 60.0 GHz band with bandwidths of 10%, gains of 6 dB and noise figures of 9 dB.

1.2 PROGRAM SUMMARY

Achievement of the above program objectives requires extensive technological advancement in the areas of InP epitaxial growth, device design and fabrication, and amplifier circuit development. During this program, significant progress has been made in each of these areas.

Two InP Gunn device structures were employed in this program, a three layer structure and a cathode notch structure. Both of these structures require several uniformly doped, high purity epitaxial layers to be grown under carefully controlled conditions. Based on a device design effort and experimental results, doping profile specifications have been established for both three layer devices and cathode notch devices for the entire frequency range from 26.5 to 60.0 GHz.

An InP vapor phase (VPE) reactor has been well characterized and yields background doping levels in the 10^{13} cm^{-3} range. An H_2S doping system and procedures have been developed which allow rapid changes in doping concentrations. During this program, both three layer wafers and cathode notch wafers were produced. Eight three layer wafers and twenty one cathode notch wafers of device quality were grown during this program. Several VPE process techniques and growth parameters have been studied in detail in an effort to establish controllability and reproducibility in the growth of InP cathode notch structures.

A well established fabrication technique which uses cleaving and ultrasonic bonding has been used to evaluate the performance of new wafers. In addition, an integral heat sink (IHS) process was developed for InP Gunn devices which

improved yield and reliability. A novel pedestal mounted packaging configuration was developed for microstrip applications.

Wideband, low noise amplification was demonstrated with InP cathode notch Gunn devices throughout 26.5-60 GHz range. With low $n\ell$ product devices ($1x10^{11}$ cm^2), noise measures of 7.7 dB were achieved in Ka-Band. Gain of 4 to 6 dB was achieved with noise figures in the 7 to 8 dB range. Devices with higher $n\ell$ products ($3\text{-}6x10^{11}$ cm^2) yielded wider band gain responses with higher gain (6 to 8 dB) with correspondingly higher noise figures (9 to 11 dB). The lowest noise measure obtained with a three layer InP Gunn device was 10.4 dB, significantly higher than the best cathode notch result.

Two amplifier circuits were developed during this program. Circuits of the coaxial-waveguide type were developed for operation up through 60 GHz. A reduced height circuit was developed for Ka-band which yielded a full band gain response from a single InP cathode notch device. The $gain^{1/2}$ bandwidth product was greater than 27 GHz.

Four final amplifier units were constructed. One for Ka-band, had a gain of 20 dB over 10 GHz bandwidth with noise figures ranging from 12.0 to 16.9 dB. Three amplifier units, having center frequencies of 43.5, 50 and 56.6 GHz, were constructed to demonstrate useful gain from an InP cathode notch device throughout the 40-60 GHz range. Gain of 6 to 8 dB and noise figures between 10.0 and 11.0 dB were achieved throughout this band. Bandwidths of all units were limited by the characteristics of available circulators.

2. DEVICE DESIGN

2.1 INTRODUCTION

The intrinsic noise measure M is used as a convenient figure of merit of the performance of a two terminal reflection amplifier.[1] The noise measure, given in equation (1), provides an assessment of the performance of the semiconductor device independent of the circuit into which it is placed.

$$M = \frac{F - 1}{1 - 1/G} \tag{1}$$

where F is the noise figure and G is the power gain of the amplifier all expressed in power ratios. From (1), the noise measure of a transferred electron device can be expressed in terms of open circuit noise voltage $\bar{V}_n^2$ across the device and the magnitude of its negative resistance $|R|$.

$$M = \frac{\bar{V}_n^2}{4kT|R|} \tag{2}$$

$\bar{V}_n^2$ and $|R|$ are functions of the diffusion coefficient D(E) and the differential negative mobility $\mu(E)$ both of which are field dependent quantities. Several workers[2,3,4] have shown that for a given bias field M will approach

$$M \rightarrow \frac{q\ D(E)}{kT\ |\mu(E)|} \tag{3}$$

at an optimum $n\ell$ product of the active layer. Figure 2.1 shows the hot electron diffusion coefficients of GaAs and InP as a function of normalized electric field.[5] The much lower diffusion coefficient of InP, at approximately twice threshold, indicates the possibility of a lower noise measure for InP than for GaAs, depending on their respective values of $\mu(E)$.

An analytical model of an InP device which assumes a uniform electric field throughout the device was used by Robson[4] to predict the noise measure of an InP transferred electron amplifier. In Figure 2.2, the noise measure derived from this model is plotted against the $n\ell$ product of the active layer of the device for three different field levels: 40, 30 and 20 kv/cm. For any given field level, as the $n\ell$ product is decreased from high values, $\bar{V}_n^2$ decreases faster with decreasing doping density than does the maximum negative resistance. However, as $n\ell$ product is lowered beyond a certain value, the small signal negative resistance begins to decrease more rapidly with decreasing $n\ell$ product as diffusion damping of space charge waves becomes significant. The minimum noise measure for a uniform field of 20 kV/cm is 2 dB and occurs at an $n\ell$ product of $5\times10^{10}cm^{-2}$. A similar calculation for GaAs indicates that its minimum noise measure is 6.5 dB at a field of 5.0 kV/cm and an $n\ell$ product of 2.4×10^{10} cm^{-2}. Thus, a significant improvement in the noise measure of a transferred electron amplifier can be expected when using InP as opposed to GaAs if the conditions of this uniform field model can be approached.

2.2 DEVICE STRUCTURES

Two InP Gunn amplifier device structures were employed in this program, a three-layer structure and a cathode-notch structure. The doping profile of a three layer structure is shown

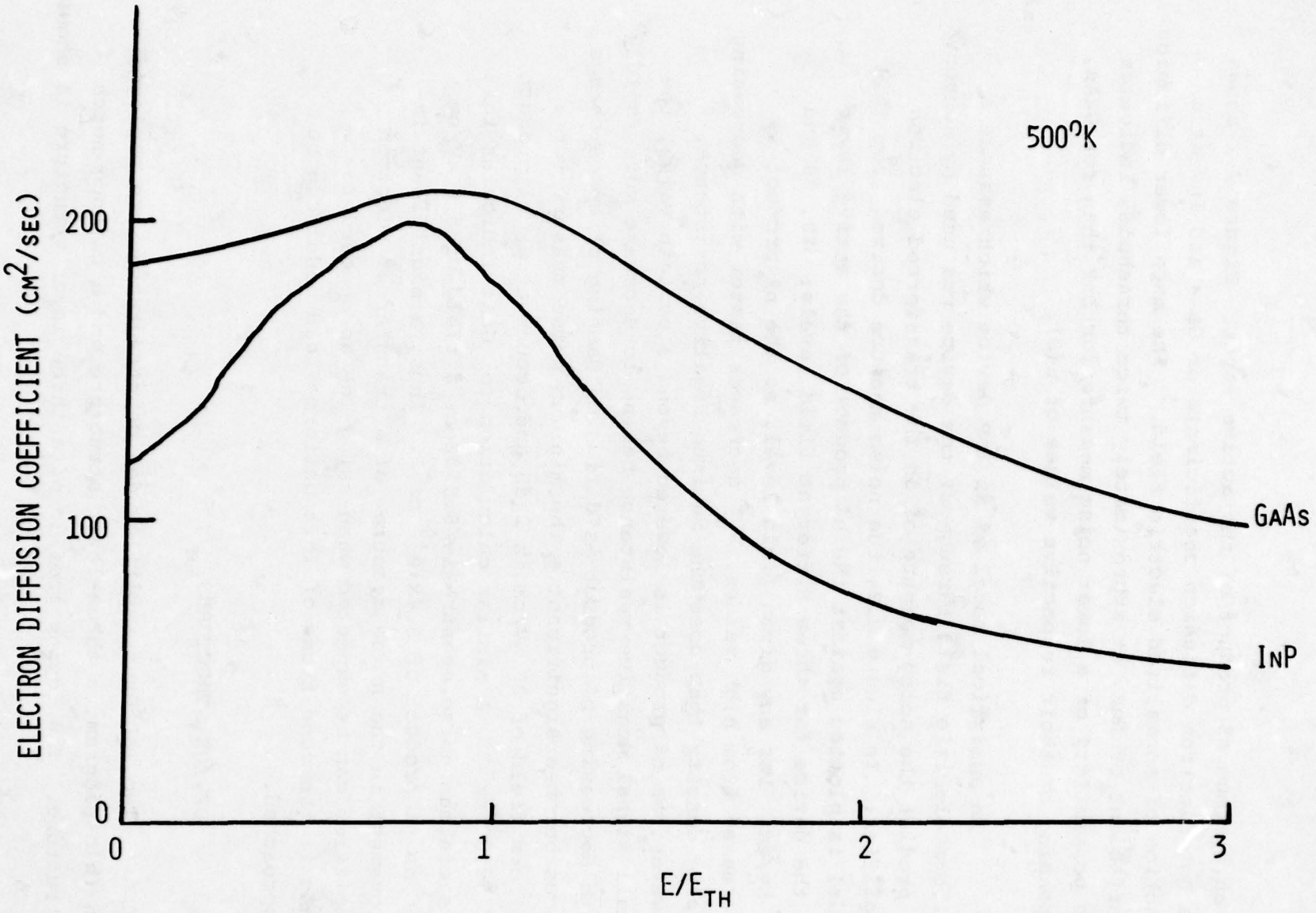


FIGURE 2.1. COMPARISON OF HOT ELECTRON DIFFUSION COEFFICIENT FOR GaAs AND InP AS A FUNCTION OF ELECTRIC FIELD

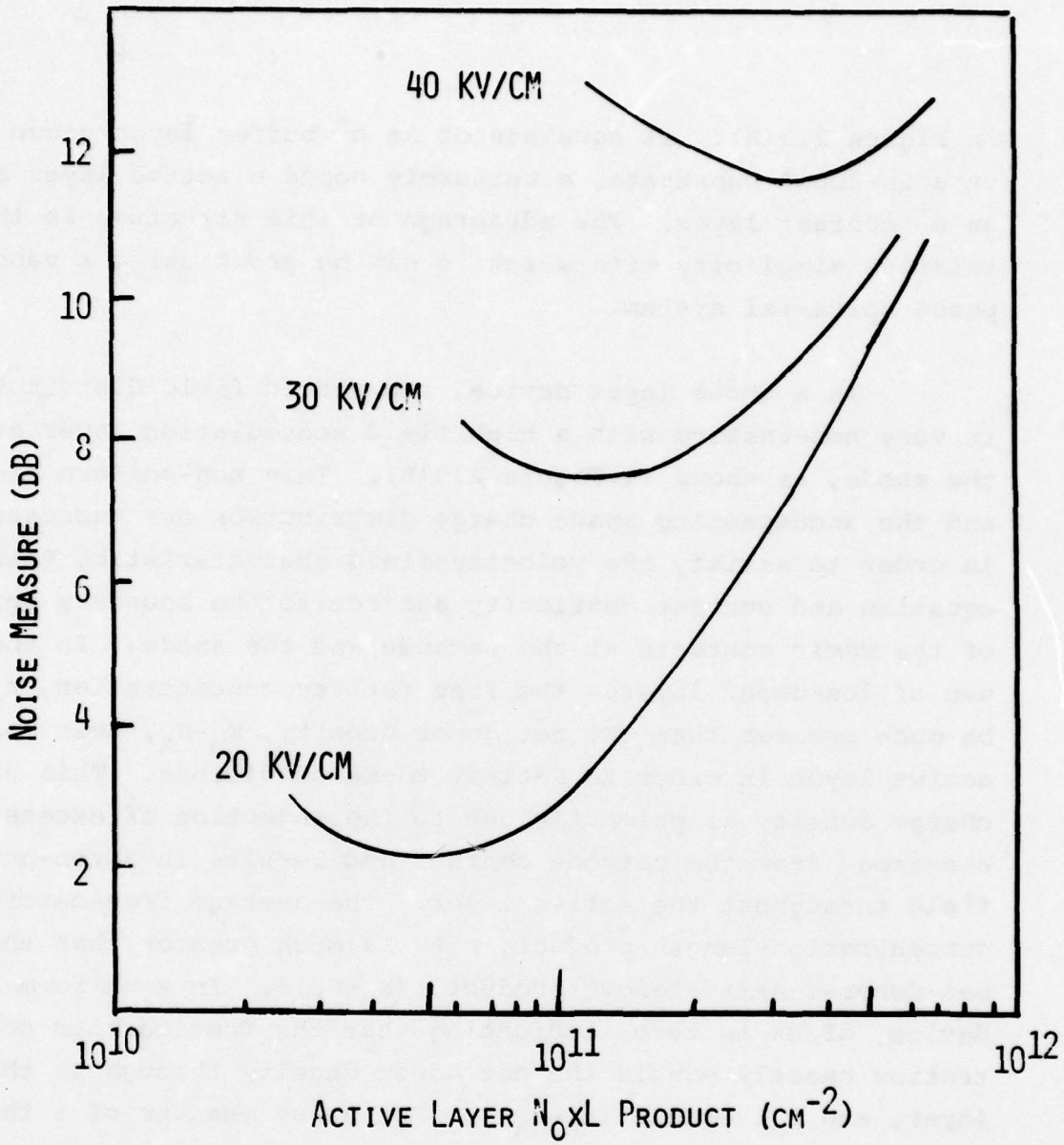
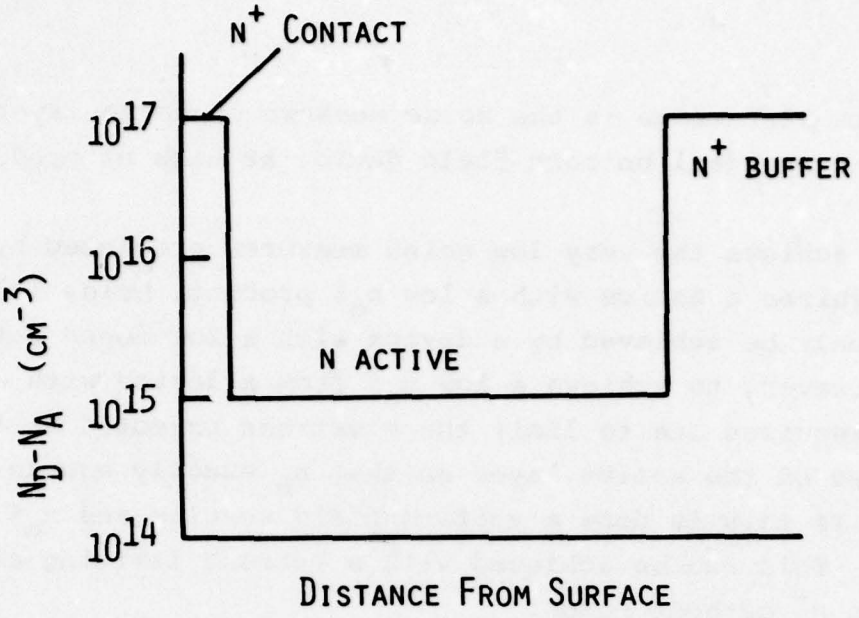


FIGURE 2.2. NOISE MEASURE AS A FUNCTION OF N_0XL PRODUCT FOR AN IDEAL UNIFORM FIELD INP T.E.A. FROM 4

in Figure 2.3(A). It consists of an n^+ buffer layer grown on a Sn-doped substrate, a uniformly doped n active layer and an n^+ contact layer. The advantage of this structure is the relative simplicity with which it can be grown using a vapor phase epitaxial system.

In a three layer device, the static field distribution is very non-uniform with a high field accumulation layer at the anode, as shown in Figure 2.3(B). This non-uniform field and the accompanying space charge distribution are necessary in order to satisfy the velocity-field characteristic, Poisson's equation and current continuity subject to the boundary conditions of the ohmic contacts at the cathode and the anode. In the use of low-doped layers, the free carrier concentration, n_o, must be much greater than the net donor density, N_D-N_A, over most of the active layer in order to satisfy these conditions. This excess charge density is primarily due to the injection of excess electrons from the cathode contact and results in a non-uniform field throughout the active layer. The average free-carrier-concentration-length product, $n_o\ell$, is much greater than the net-donor-density-length product, $(N_D-N_A)\ell$. In a uniform field device, dE/dX is zero, indicating that the free carrier concentration exactly equals the net donor density throughout the active layer, and $n_o\ell$ equals $(N_D-N_A)\ell$. The noise measure of a three layer device with a low $(N_D-N_A)\ell$ product is therefore significantly higher than that of a uniform field device with the same $(N_D-N_A)\ell$ product. At higher $n\ell$ product, the excess injected space charge is not as significant and the free carrier concentration is approximately equal to the donor density throughout most of the active layer. Therefore, there is no



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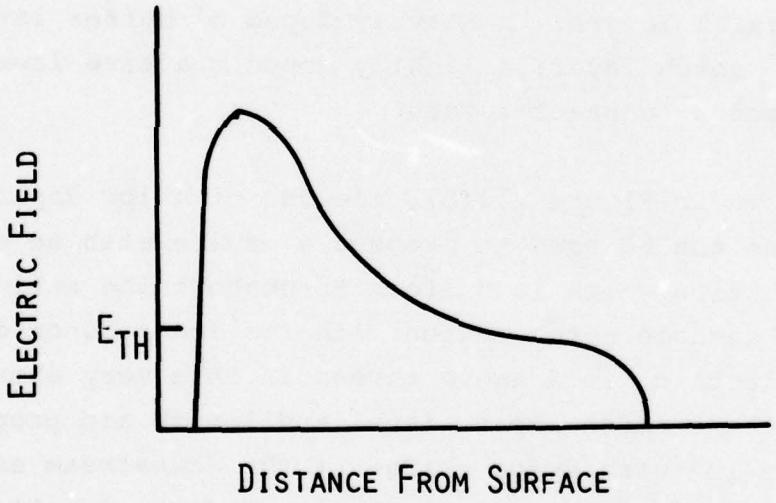


(B)

FIGURE 2.3 INP THREE LAYER STRUCTURE

(A) IDEALIZED DOPING PROFILE

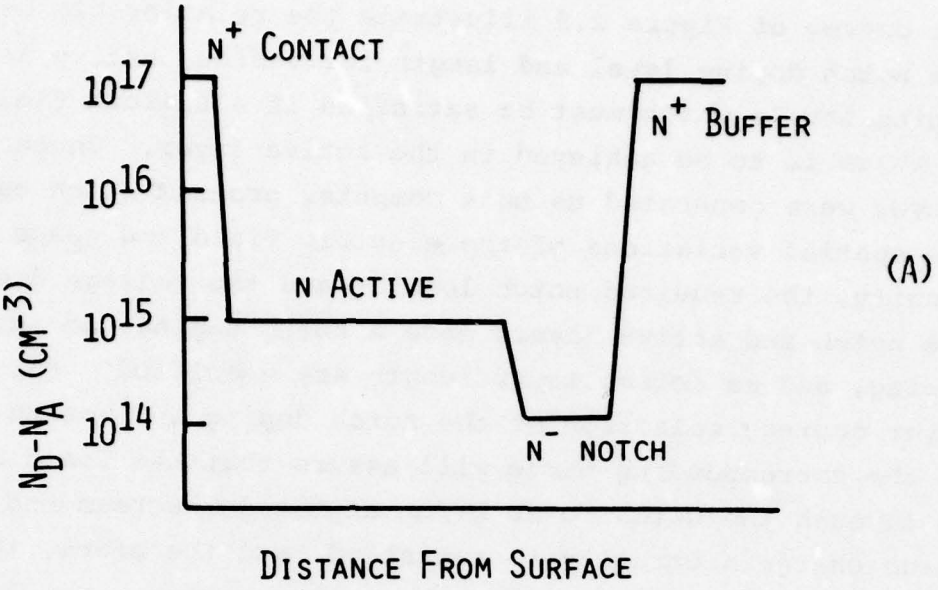
(B) TYPICAL ELECTRIC FIELD DISTRIBUTION

appreciable difference in the noise measure of three layer devices and an ideal uniform field device at high $n\ell$ products.

To achieve the very low noise measures predicted by Robson requires a device with a low $n_o\ell$ product, below $1x10^{11}$ cm^{-2}. This can only be achieved by a device with a low doped active layer. However, to achieve a low $n_o\ell$ from a device with a low $(N_D-N_A)\ell$ requires one to limit the electrons injected at the cathode end of the active layer so that n_o exactly equals (N_D-N_A). If this is done a uniform field results and $n_o\ell$ equals $(N_D-N_A)\ell$. This can be achieved with a current limiting cathode, such as an n^- cathode notch.

The idealized doping profile of an InP cathode notch structure is shown in Figure 2.4(A) as well as a typical electric field profile. The cathode notch structure consists of four epitaxial layers: a heavily doped n^+ buffer layer; an undoped n^- notch layer; a lightly doped n active layer; and, a heavily doped n^+ contact layer.

As shown in Figure 2.4(B), the use of a low doping notch at the cathode can be used to produce a device with an electric field distribution which is uniform throughout the active region. The cathode notch region with its lower donor density drives the electric field above threshold in a very short distance. If the notch doping level and length are properly selected, the injected space charge at the downstream end of the notch can be forced to equal the fixed donor density, achieving space charge neutrality and uniform electric field across the active region.



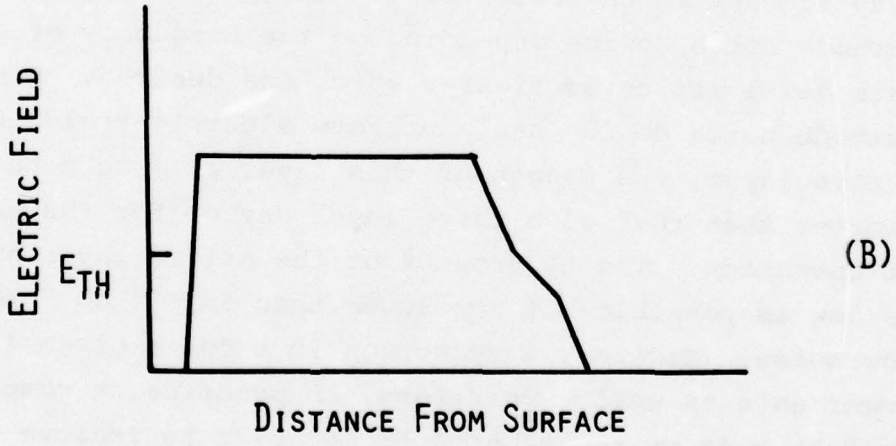


FIGURE 2.4 INP CATHODE NOTCH STRUCTURE

(A) IDEALIZED DOPING PROFILE

(B) TYPICAL ELECTRIC FIELD DISTRIBUTION

The curves of Figure 2.5 illustrate the relationship between the notch doping level and length for various active layer doping levels which must be satisfied if a uniform field of 20 kV/cm is to be achieved in the active layer. These curves were generated using a computer program which calculates the spatial variations of the electric field and space charge density, the required notch length, and the voltage drops across the notch and active layers once a notch doping, an active layer doping, and an active layer length are specified. For a given active layer doping, selection of the notch doping and length which fall on the corresponding curve will assure that the field builds up through the notch to 20 kV/cm at the downstream end and that space charge neutrality is satisfied, and therefore, that a uniform field will result in the active region. Notch design curves have been generated for active layer doping levels ranging from $6 \times 10^{14} cm^{-3}$ to $2 \times 10^{15} cm^{-3}$.

There are several important factors which must be taken into account in the selection of the profile parameters of a cathode notch device depending on the frequency of operation, the gain level and noise figures which are desired. Since a cathode notch device has a uniform electric field in the active layer, the length of this layer will be considerably shorter than that of a three layer device for the same frequency of operation. The $n\ell$ product of the active layer should be as low as possible but not lower than $5 \times 10^{10} cm^{-2}$ to achieve low noise. However, a reduction in n for a given ℓ results in lower gain as well. Therefore, in practice, a compromise must be made on the $n\ell$ product in order to achieve low noise with a reasonable gain level. The notch parameters for a specific uniform field in the active layer are independent of the active layer length; they are dependent only on the active layer doping level. As the active layer doping is decreased

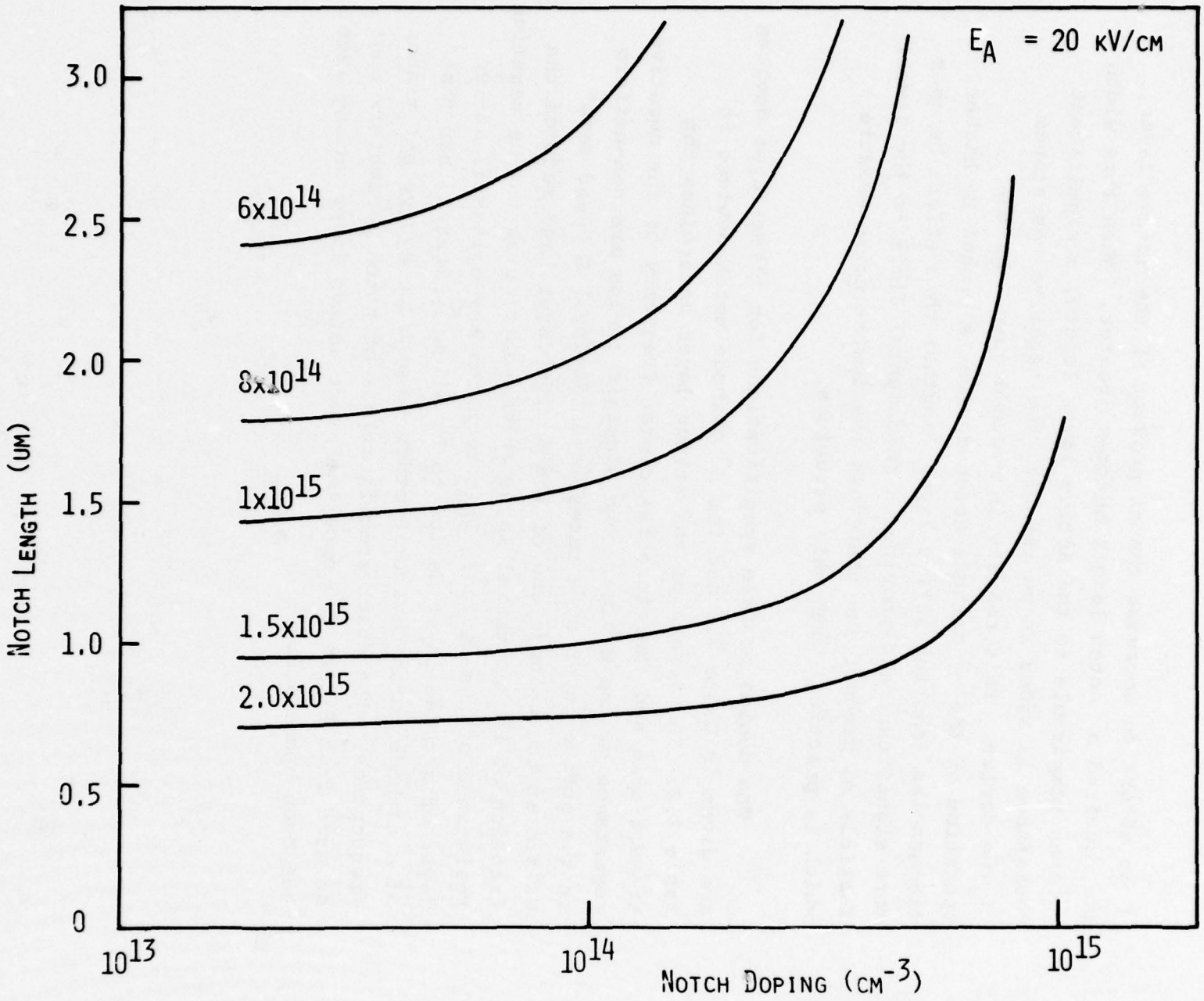


FIGURE 2.5 NOTCH DOPING VERSUS LENGTH FOR SPECIFIC ACTIVE DOPINGS

in an effort to decrease the $n\ell$ product of the active layer, the required n^- notch length becomes greater. When this width becomes comparable to the active layer length, a significant resistance is added in series with the negative resistance of the device. This results in reduced gain. As the operation of the n^- cathode notch device is pushed to higher frequencies (shorter active layer lengths) this effect becomes more significant and provides a fundamental limit to the lowest feasible $n\ell$ product and therefore the lowest noise measure which is practical with this structure.

The doping profile specifications for three-layer devices are given in Table 2.1 and for n^- cathode notch devices in Table 2.2. The length of the active layer determines the transit time and therefore the center frequency of the negative resistance of the device. The electric fields are non-uniform in the active layer of a three layer device. A "dead zone" exists at the cathode end of the active layer, and reduces the fraction of the epitaxial layer which contributes to the negative resistance of the device. This requires the epitaxial active layer of a three layer device to be slightly longer than that of a cathode notch device in order to produce equivalent transit frequencies. The exact specifications of notch parameters must be made from Figure 2.5 once the exact active layer doping level has been specified.

TABLE 2.1

DOPING PROFILE SPECIFICATIONS FOR THE
ACTIVE LAYER OF AN InP THREE LAYER STRUCTURE

	ACTIVE LAYER	
F (GHz)	Doping (cm^{-3})	Length (μm)
26.5-40	$.6\text{-}.8 \times 10^{15}$	4.0-5.0
40-60	$.8\text{-}1.0 \times 10^{15}$	3.0-4.0

TABLE 2.2
DOPING PROFILE SPECIFICATIONS FOR AN InP
N^- CATHODE NOTCH STRUCTURE

	NOTCH LAYER		ACTIVE LAYER	
F (GHz)	DOPING (cm^{-3})	LENGTH (μm)	DOPING (cm^{-3})	LENGTH (μm)
26.5-40	$.3\text{-}.5 \times 10^{14}$	1.7-2.5	$.6\text{-}.8 \times 10^{15}$	3.5-4.5
40-60	$.3\text{-}.5 \times 10^{14}$	1.4-1.8	$.8\text{-}1.0 \times 10^{15}$	2.0-3.5

3. VAPOR PHASE EPITAXIAL GROWTH OF InP

3.1 INTRODUCTION

Epitaxial InP layers for Gunn amplifiers operating in the millimeter range were grown by the chloride passport process utilizing a saturated In source. The $In/PC\ell_3/H_2$ VPE process used was first described by Clarke et al.[6] and has been developed further at Varian.[7] This work has now been extended to improve the material growth process in order to obtain reproducible growth rates, good interface quality and precise doping control that are necessary in the growth of three layer and cathode notch structures. High purity material is obtained by maintaining an oxygen free, leak tight system. The reactor is fabricated from high purity spectrosil quartz. Palladium diffused H_2 is used and both $PC\ell_3$ and In are of 6-9's purity.

3.2 InP VPE REACTOR

A schematic of the VPE InP reactor is shown in Figure 3.1. The reactor design is very similar to the $AsC\ell_3$, Ga, H_2 system used in VPE GaAs. All gas flows are controlled with mass flow controllers (MFC) and the $PC\ell_3$ mole fraction is controlled with a constant temperature condenser bubbler and MFC gas flow control. The reactor furnace is rolled on and off the reactor tube during each VPE deposition.

The reactor is purged with N_2 with the furnace in the off position for loading and unloading wafers. $PC\ell_3$ can be passed either over the indium source or between the source and deposition zone or both. This allows vapor etching of reactor wall deposits or wafers during a deposition process.

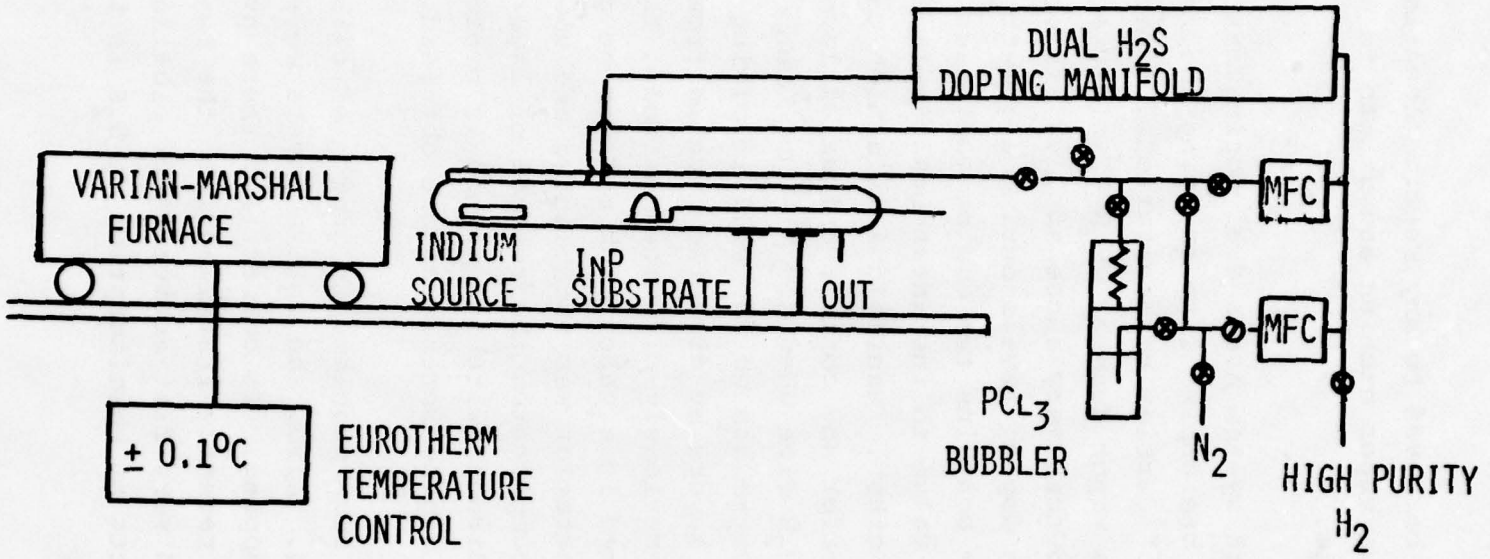


FIGURE 3.1. VAPOR EPITAXIAL InP REACTOR

Wafers can also be moved to any reactor location during a run. This allows vapor etching and growth to occur where it is most desirable.

The growth system has a dual doping manifold shown in Figure 3.2 with one doping line entering the reactor. Except for low 10^{14} cm^{-3} carrier concentrations, doping is best obtained using a vapor dopant. H_2S/H_2 mixtures have been used as the dopant sources very successfully. In order to make rapid changes in doping levels during a growth, the dopant gas injection system contains two doping manifolds and a zero dead volume four way valve to instantaneously switch from one manifold to the other. Manifold A is a high ppm H_2S line used for 10^{17} cm^{-3} buffer and contact epitaxial layers. Manifold B is a low ppm H_2S line used for 10^{15} cm^{-3} range active Gunn layers. This system has worked well in giving the desired doping changes between layers by direct switching from one manifold to the other. Previously with one manifold, the epitaxial process was placed in a vapor etch mode or no growth mode while a new H_2S concentration was established and then growth was resumed. This complicates the control of layer thickness. Therefore, the direct switching method is preferred as long as clean, sharp doping interfaces are obtained.

However, some problems in growth of cathode notch structures were encountered. Also, the active layers were often found to have graded doping. To correct for these problems, a second doping line was recently installed into the reactor for low level doping and very flat active layer profiles are now being obtained. Effects of chemisorption of H_2S in the quartz lines is described later.

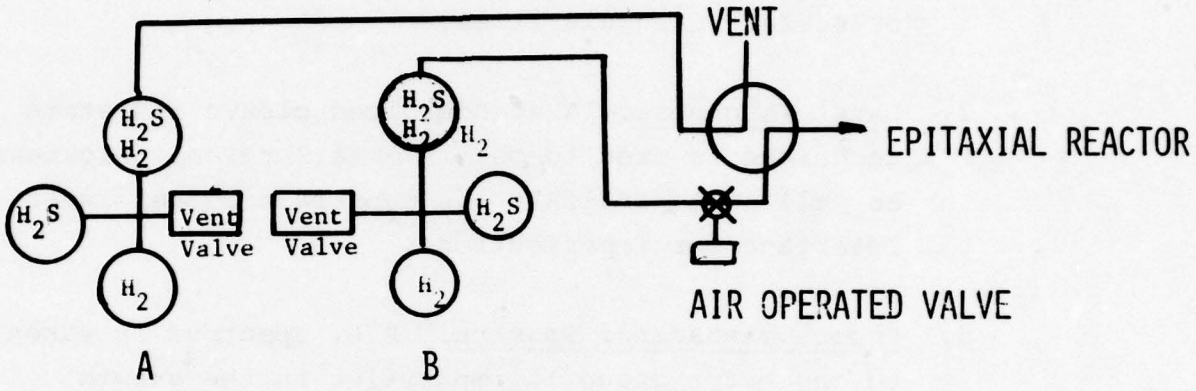


FIGURE 3.2. DIAGRAM OF DUAL DOPING MANIFOLD

3.3 MATERIAL CHARACTERIZATION

The VPE wafers are characterized as follows:

1. Surface Quality. The texture and flatness are determined by optical microscopy using Nomanski interference contrast to reveal any minor defects or surface irregularities.

2. Layer Thickness. A standardized cleave and stain technique is used to obtain metallurgical thickness as well as to evaluate the substrate/buffer layer interface for imperfections.

3. Photoluminescence Spectra. P.L. spectrum is taken to check for group II impurities in the growth. Such impurities can be present in the source or substrate.

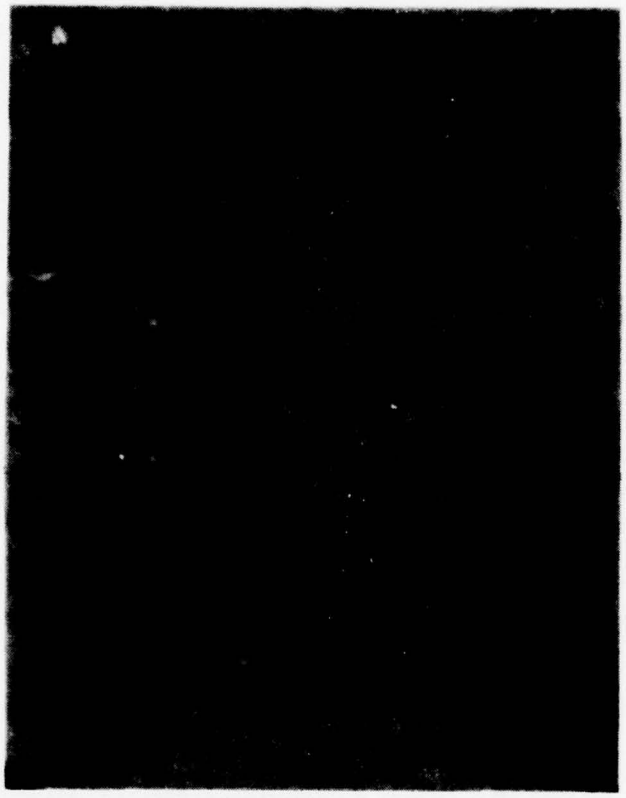
4. Schottky Barrier Impurity Profiling. Carrier concentration profiles vs depth are obtained from C-V measurements at $77^{o}K$. A sample test wafer from every run is evaluated. The first profile obtained on a wafer only gives the contact layer doping because voltage breakdown occurs in the contact layer. Therefore, the samples are etched to remove the contact layer, new Schottky diodes are evaporated and a second profile showing the active layer is obtained. Additional etching and reprofiling is continued until a complete profile of all the layers is obtained.

5. Hall Measurements. Van der Pauw Hall measurements were made to determine Hall mobility and carrier concentrations at room temperature and 77°K. This is done on the first deposition with each indium source to insure reactor background purity. High mobility indicates low compensation levels and higher purity.

Figure 3.3 shows a low magnification optical surface micrograph of a three layer InP growth on Sn-doped (100) InP substrate. Figure 3.4 is the cleaved section of a three layer wafer after a stain-etch in a $KOH:KFe(CN)_6$ solution.[8] The photograph taken at x1400 magnification clearly shows the metallurgical thickness of each of the layers. This process is routinely used to determine the thickness of the grown layers.

Photoluminescence spectra are taken to check for zinc, Cd or Hg impurities present in the source. Figure 3.5 shows the PL spectrum of a growth with compensating impurity and one without. Use of AlA indium from Johnson-Matthey Company has normally given PL spectra with low zinc peaks.

A plot of Van der Pauw Hall mobility vs net carrier concentration is shown in Figure 3.6. This is a good method of evaluating material purity as high mobilities indicate low compensation levels. Additional data from Plessey and RRE are included for comparison. The highest mobilities measured on Varian material were 6060/140,220 cm^2/v-sec at 300°K/77°K for a $6x10^{13}$ cm^{-3} layer. Typically high quality low 10^{15} cm^{-3} layers have 300°K/77°K mobilities of 4600-5200/40,000-60,000 cm^2/v-sec. In addition, low carrier concentration freeze-out



440X

FIGURE 3.3 OPTICAL SURFACE MICROGRAPH OF A THREE LAYER InP WAFER

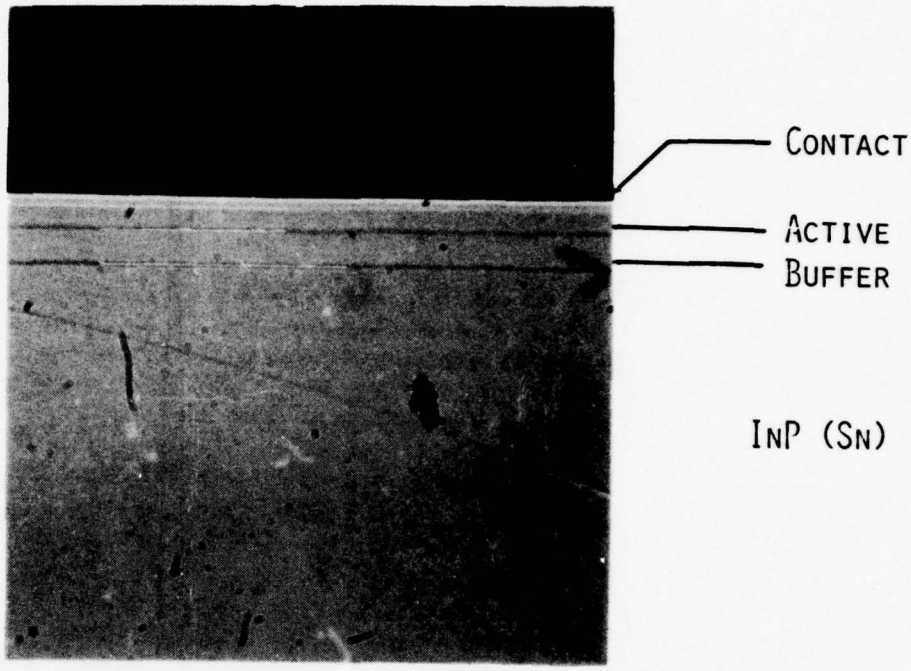


FIGURE 3.4. CLEAVED AND STAINED CROSS SECTION SHOWING THE EPITAXIAL LAYERS OF AN INP THREE LAYER DEVICE.

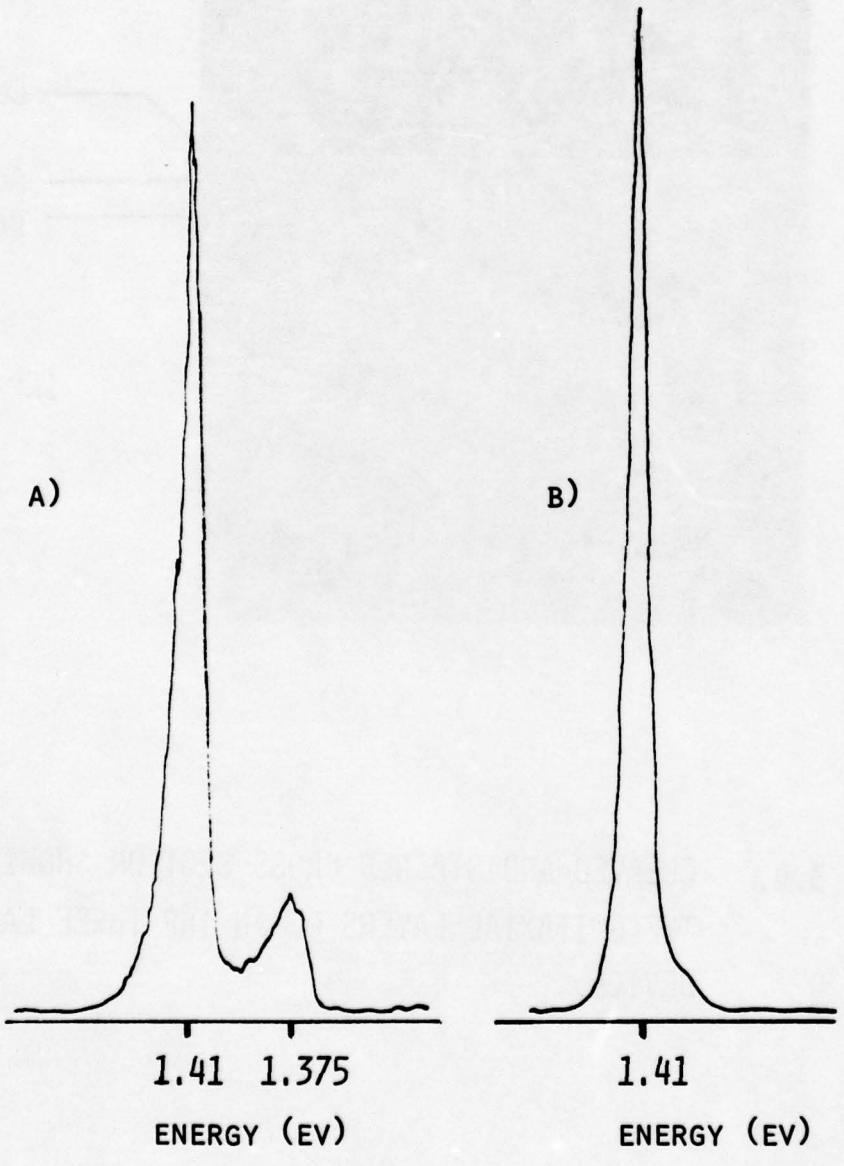


FIGURE 3.5 PHOTOLUMINESCENCE SPECTRA OF InP EPITAXIAL LAYERS GROWN WITH (A) AND WITHOUT (B) COMPENSATING IMPURITIES

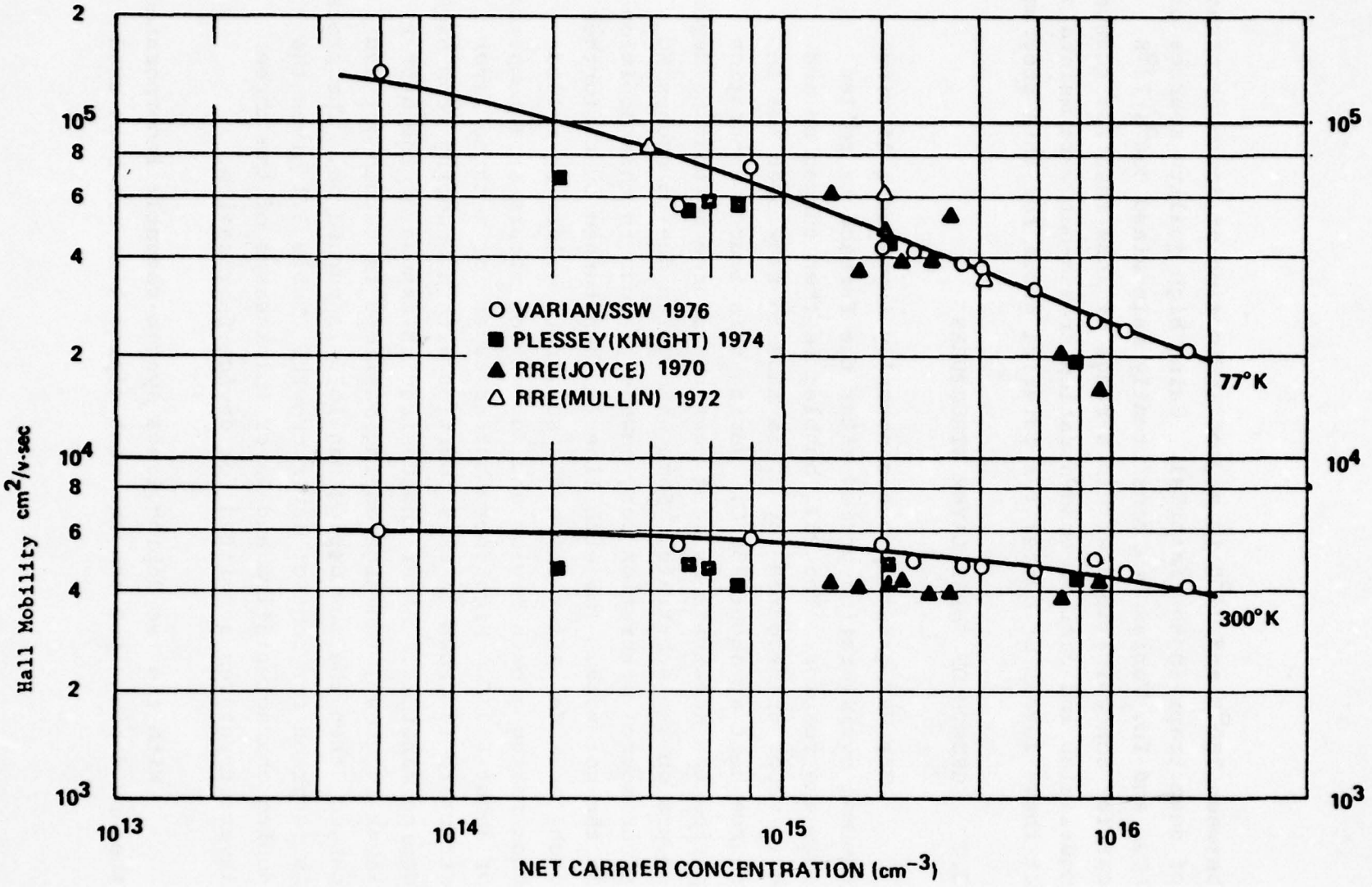


FIGURE 3.6 HALL MOBILITY VS NET DOPING CONCENTRATION

between 300°K and 77°K is a good indication of low concentrations of deep traps in the material. Using high quality sources of $PC\ell_3$ and In, Varian has consistently maintained 300°K/77°K carrier concentrations within a range of less than 20% change. Mobilities and carrier concentration freeze-out were maintained at these levels or better for material grown for this program.

3.4 GROWTH OF THREE LAYER STRUCTURES

The VPE growth process normally involves a 15 minute thermal equilibration period after the furnace is rolled onto the reactor. The $PC\ell_3$ bubbler is then turned on and $PC\ell_3$ vapor transported by H_2 is made to flow over the In source kept at about 750°C. During this source saturation period the substrate is kept near the source so that no deposition occurs on the substrate. Some wafer etch due to excess HC after source saturation can, however, occur in this position in the hot zone. The etch line is then turned on to further etch the wafer after which the substrate holder is pulled back in the growth region and deposition occurs at a temperature of about 650°C. High doped buffer layer for a three layer structure is grown in this position with H_2S doping from high doping manifold. After the desired thickness of the buffer layer is grown, the high doping manifold is turned off and purged, then the low doping manifold is turned on. The process is reversed for contact layer growth. Table 3.1 gives the doping characteristics and layer thicknesses of the three layer structures submitted for device fabrication.

With the two doping lines system recently incorporated the low doping line and the high doping line are both used

TABLE 3.1

VPE InP FLAT PROFILE WAFERS

SSW RUN NO.	EPITAXIAL LAYERS					
	BUFFER N^+		ACTIVE N		CONTACT N^+	
	N (cm^{-3})	T (μm)	N (cm^{-3})	T (μm)	N (cm^{-3})	T (μm)
44-3	$1.9x10^{17}$	3.5	$7x10^{15}$	4.1	$1.9x10^{17}$	0.5
44-4	$2.3x10^{17}$	3.1	$6x10^{15}$	3.2	$2.3x10^{17}$	0.7
44-5	$5.0x10^{16}$	1.5	$2x10^{15}$	3.2	$1.0x10^{17}$	1.1
46-12	$5.5x10^{16}$	4.6	$7.5x10^{14}$	6.1	$5.5x10^{16}$	0.9
47-3	$9x10^{16}$	3.0	$2.0x10^{15}$	4.7	$9x10^{16}$	0.9
47-4	$1.5x10^{17}$	3.3	$1.0x10^{15}$	6.2	$1.5x10^{17}$	0.6
47-7	$2.3x10^{17}$	5.3	$2.3x10^{15}$	5.1	$2.3x10^{17}$	0.6
49-6	$1.8x10^{17}$	4.6	$2.1x10^{15}$	7.0	$1.8x10^{17}$	0.7

for buffer and contact layer growth. The active layer is grown by shutting off the high doping line. This procedure was adopted since the low doping line with 10^{-3} ppm H_2S would desaturate due to chemisorption of H_2S in the quartz if the line is shut off. A three layer structure grown by this process using the two line system yields a very flat active layer profile as shown in Figure 3.7 as compared to that grown with a single doping line, in which case doping gradients are often observed in the active layer.

3.5 GROWTH OF CATHODE NOTCH STRUCTURES

The procedure for the growth of cathode notch structures was similar to that for three layer structures, except that for notch growth, the doping line was purged and shut off completely so that undoped, background doping level growth occurred. The low doping manifold was then turned on to obtain the active layer at the end of which the contact layer was grown with high doping again. Tables 3.2 and 3.3 give the doping levels and thicknesses of the cathode notch wafers grown in this manner. Figures 3.8 through 3.11 show some of the typical profiles obtained. Purging times of the H_2S doping line after the buffer layer growth were found to be critical in obtaining a flat active layer profile and symmetrical notch profile, and reproducibility of results was difficult. To avoid this some growth runs were made with the substrate ahead of the H_2S inlet during notch and active layer growth, the active layer doping being achieved by back diffusion of H_2S. Higher H_2S ppm could be used in this situation allowing better flow control. The results for the three growth runs made this way are shown in Table 3.4.

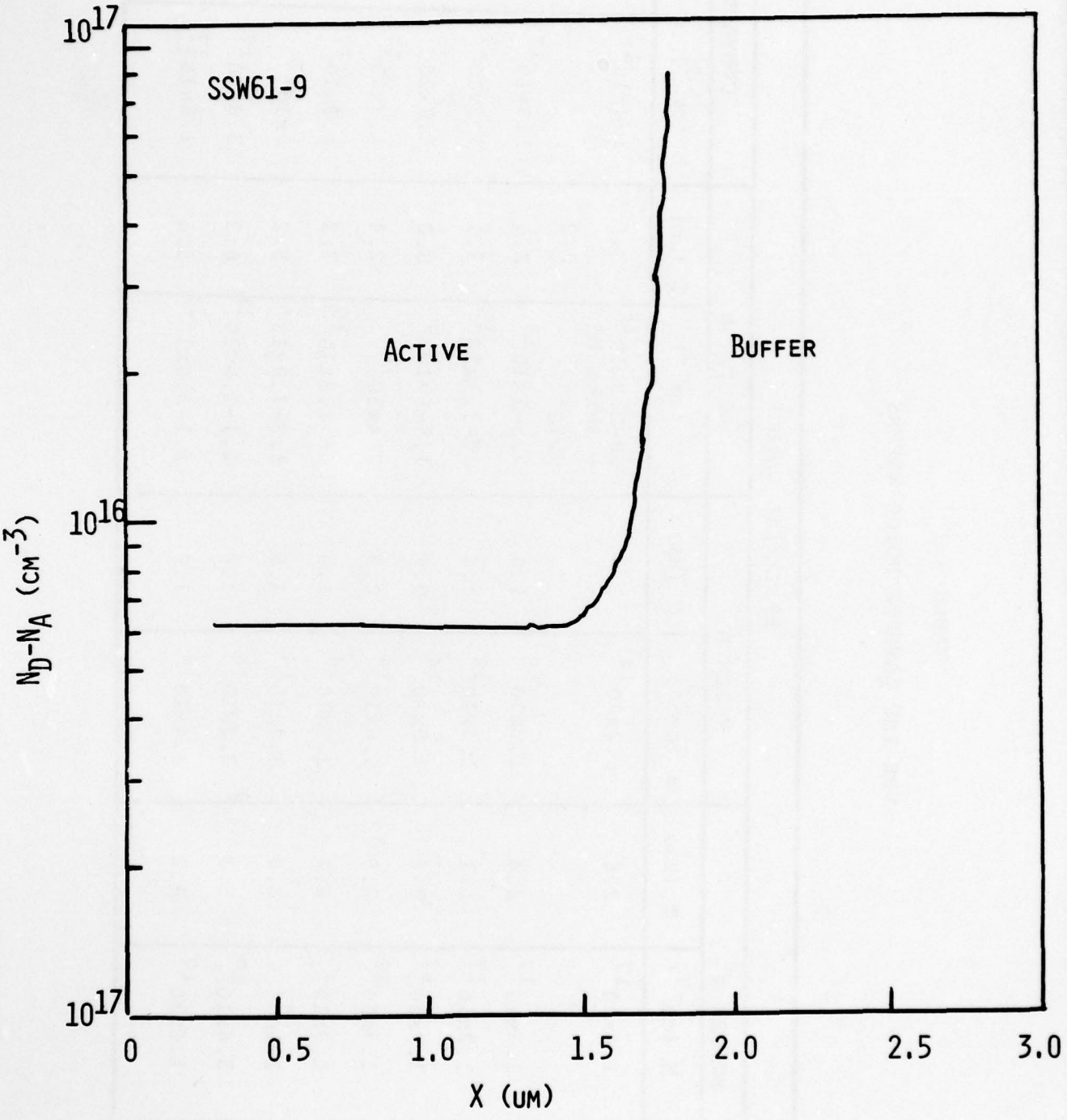


FIGURE 3.7. C-V PROFILE OF INP THREE LAYER WAFER SSW61-9

TABLE 3.2

VPE InP CATHODE NOTCH WAFERS

RUN NO.	EPITAXIAL LAYERS							
	BUFFER N^+		NOTCH N^-		ACTIVE N		CONTACT N^+	
	N (cm^{-3})	T (μm)	N (cm^{-3})	T (μm)	N (cm^{-3})	T (μm)	N (cm^{-3})	T (μm)
47-8	$1.4x10^{17}$	2.6	$6.2x10^{14}$	1.4	$.8\text{-}2.8x10^{15}$ + spike to $5x10^{16}$	3.1 0.2	$1.4x10^{17}$	.46
47-9	$1.3x10^{17}$	2.4	$1.2x10^{15}$	1.0	$2.5\text{-}3x10^{15}$	2.3	$1.3x10^{17}$	.40
48-1	$1.2x10^{17}$	5.1	$1.4x10^{14}$	1.6	$.7\text{-}1.1x10^{15}$	3.1	$1.2x10^{17}$	.57
48-2	$1.7x10^{17}$	2.6	$5.8x10^{14}$	0.9	$1.5\text{-}5x10^{15}$	3.0	$1.7x10^{17}$	.50
48-4	$1.7x10^{17}$	2.5	$5.6x10^{14}$	0.9	$2\text{-}4x10^{15}$	2.4	$1.7x10^{17}$	.57
48-7	$1.3x10^{17}$	2.7	$2.5x10^{14}$	1.3	$.6\text{-}1.2x10^{15}$	3.2	$1.3x10^{17}$	.71
50-2	$2x10^{17}$	3.4	$8.4x10^{14}$	1.5	$1.3\text{-}3.9x10^{15}$	5.2	$2x10^{17}$	.50
51-2	$3.8x10^{17}$	5.3	$3.2x10^{14}$	1.8	$1.1\text{-}1.6x10^{15}$	6.2	$3.8x10^{17}$	.93
51-3	$1.6x10^{17}$	4.2	$2.4x10^{14}$	1.6	$1.1\text{-}2.0x10^{15}$	5.0	$1.6x10^{17}$	1.0

TABLE 3.3

VPE InP CATHODE NOTCH WAFERS*

RUN NO SSW	N^+ BUFFER		N^- NOTCH		N ACTIVE		N^+ CONTACT		$PC\ell_3$ MOLE FRACTION†
	N (cm^{-3})	T (μm)	N (cm^{-3})	T (μm)	N (cm^{-3})	T (μm)	N (cm^{-3})	T (μm)	
52-9	1.0e17	3.0	4.8e13	2.4	9.0e14	3.2	1.0e17	1.0	4.0×10^{-2}
53-2	2.1e17	2.9	2.0e14	1.7	2.5e15	3.9	2.1e17	1.0	9.23×10^{-3}
53-4	1.5317	3.4	5.1e13	1.7	1.4e15	4.6	1.5e17	1.0	4.0×10^{-2}
53-5	1.3e17	3.5	3.2e13	2.5	6.0e14	3.9	1.3e17	1.3	4.0×10^{-2}
53-6	1.4e17	3.8	3.1e13	2.8	1.0e15	2.1	1.4e17	1.5	4.0×10^{-2}
53-7	1.7e17	3.3	6.2e13	1.7	8.2e14	2.3	1.7e17	1.0	4.0×10^{-2}
54-3	1.4e17	.34	2.0e14	1.0	9.4e14	0.7	1.4e17	0.9	4.0×10^{-2}
54-5	1.3e17	3.0	5.6e13	1.8	1.2e15	1.8	1.3e17	1.1	4.0×10^{-2}
54-7	1.6e17	2.9	7.7e13	1.5	1.8e15	1.7	1.6e17	1.3	4.0×10^{-2}
54-8	1.5e17	3.6	1.1e14	1.6	1.1e15	1.7	1.5e17	1.3	4.0×10^{-2}
54-9	1.6×10^{17}	3.2	5.7×10^{13}	1.8	3.4×10^{14}	2.4	1.6×10^{17}	1.3	4.0×15^{-2}

* Measurements at $77^{\circ}K$

† Mole fraction for undoped notch layer. The mole fraction is slightly lower for doped layers where additional H_2S/H_2 is added to the reactor thereby causing $PC\ell_3$ dilution.

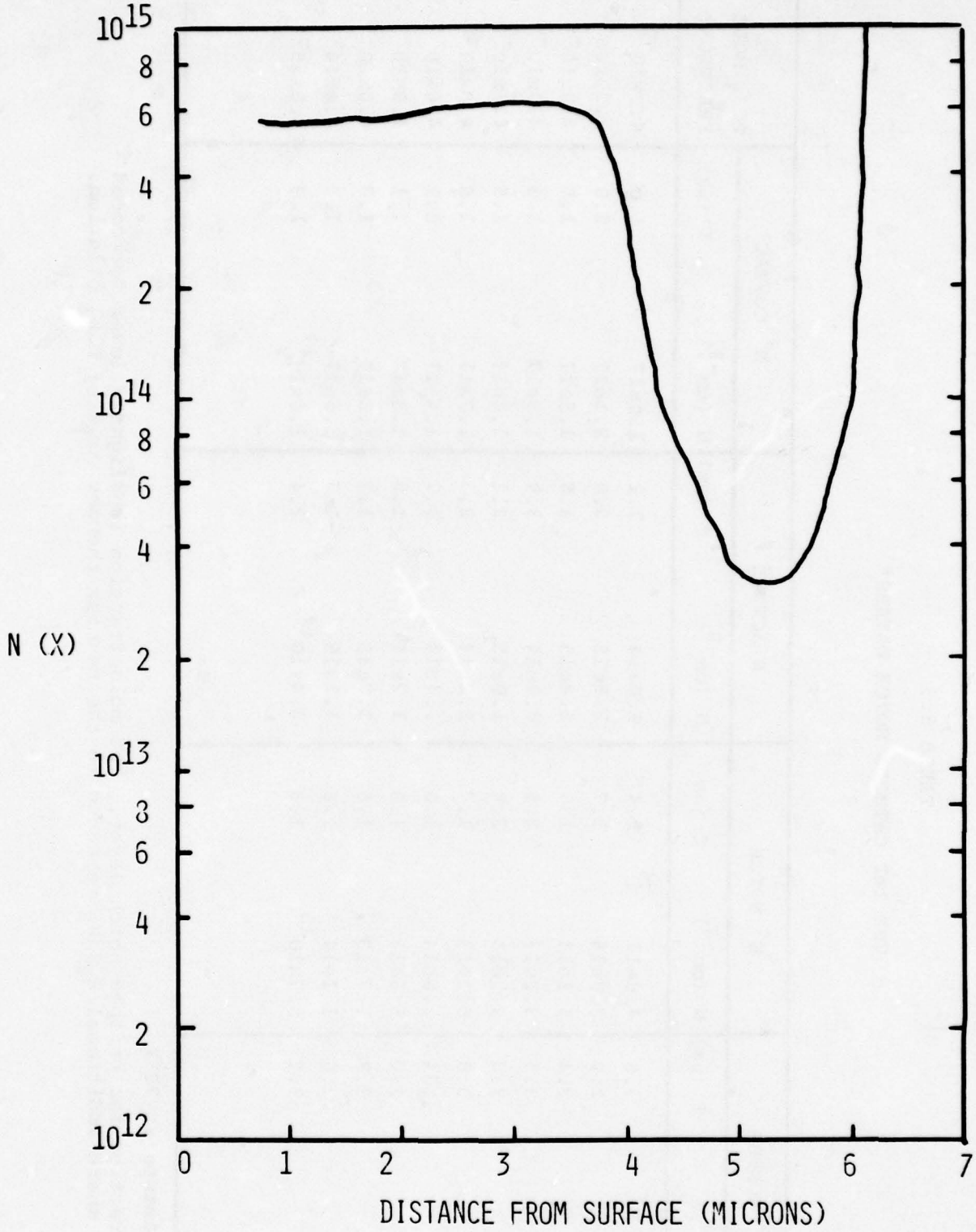


FIGURE 3.8 InP VPE SSW53-5T_1

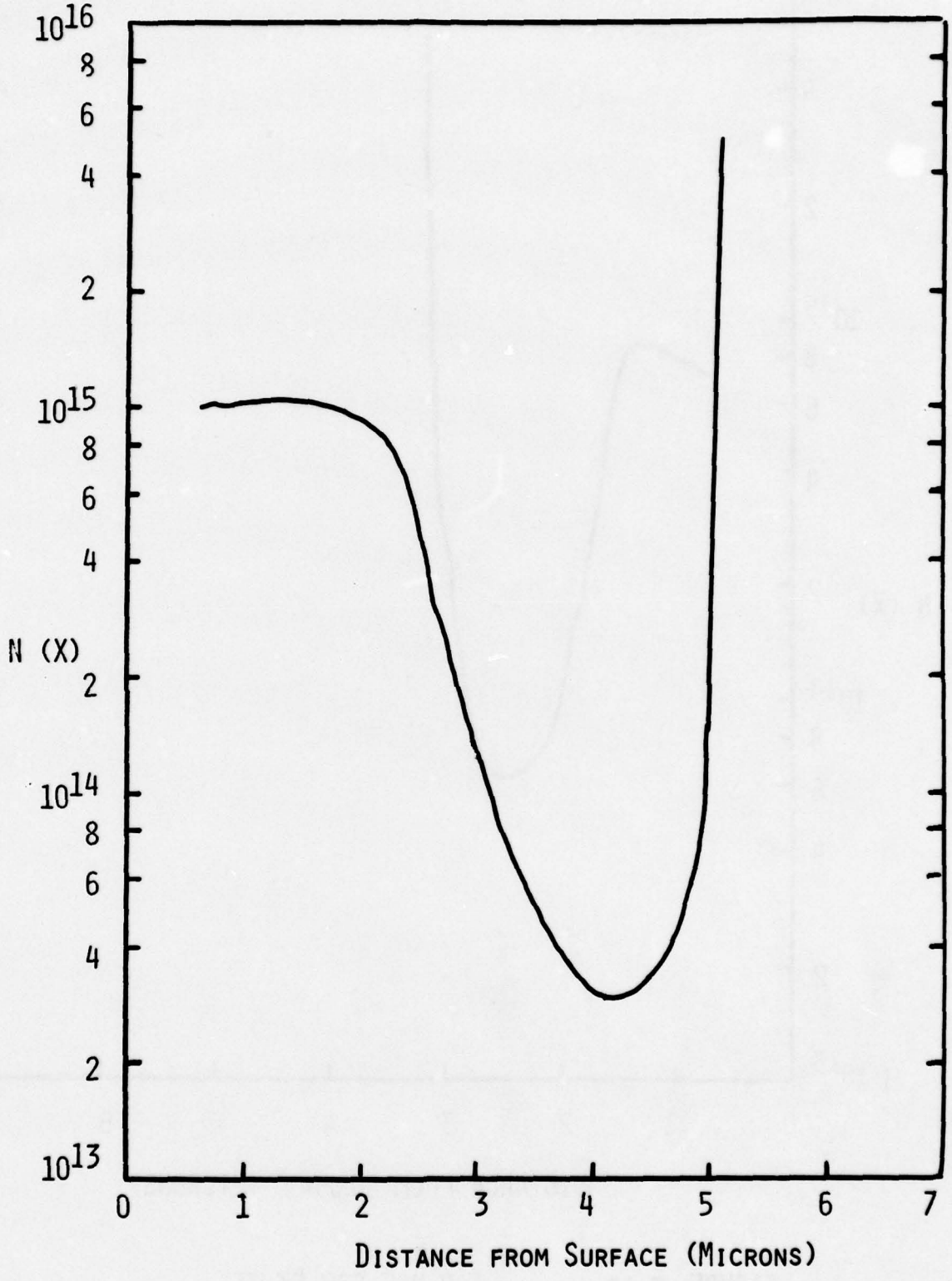


FIGURE 3.9. InP VPE SSW 53-6T_1

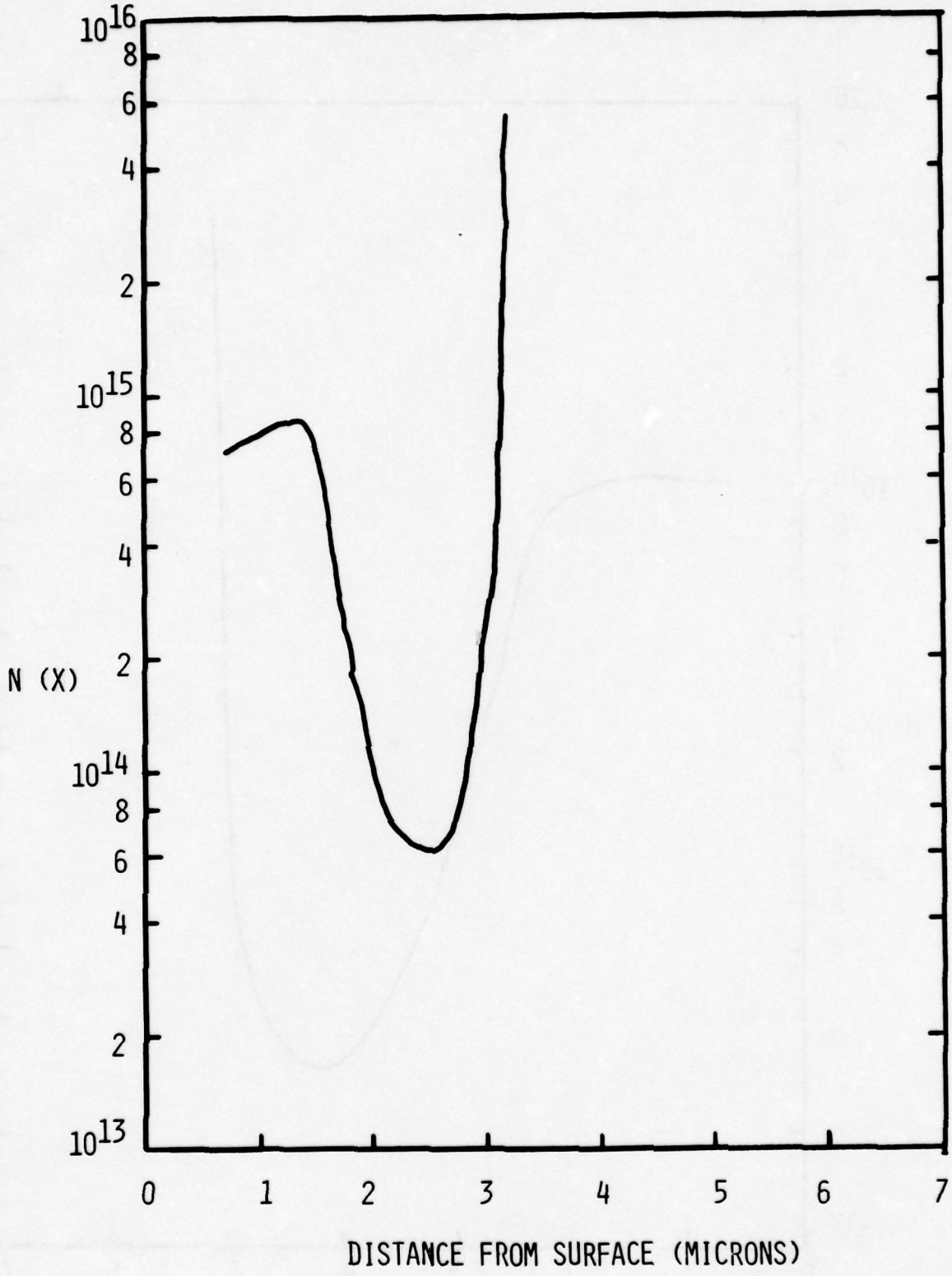


FIGURE 3.10 InP VPE SSW 53-7T_1

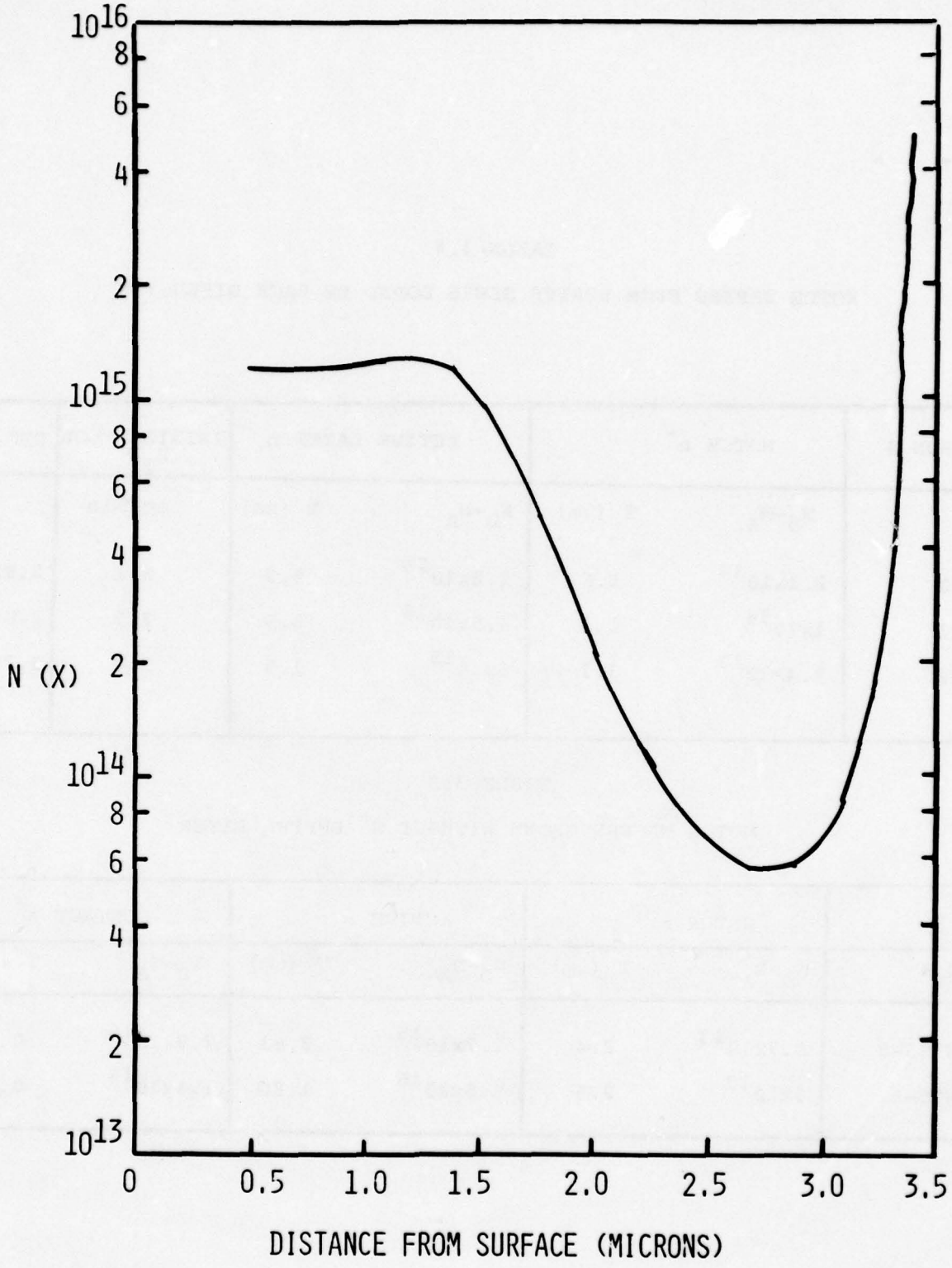


FIGURE 3.11 InP VPE SSW $54\text{-}5T_1$

TABLE 3.4

NOTCH WAFERS FROM SERIES SSW55 DOPED BY BACK DIFFUSION

SSW RUN #	NOTCH n^-		ACTIVE LAYER n		INITIAL FLOW H_2S	ppm H_2S
	N_D-N_A	T (μm)	N_D-N_A	T (μm)	cc/min	
54-10	2.1×10^{14}	1.6	2.2×10^{15}	5.2	8.1	5.98×10^{-2}
54-11	1×10^{14}	1.3	4.5×10^{14}	3.5	2.7	2.01×10^{-2}
54-12	2.4×10^{13}	3.1	5×10^{15}	1.5	3.7	2.75×10^{-2}

TABLE 3.5

NOTCH WAFERS GROWN WITHOUT N^+ BUFFER LAYER

	NOTCH n^-		ACTIVE n		CONTACT n^+	
RUN #	N_D-N_A	T (μm)	N_D-N_A	T (μm)	N_D-N_A	T (μm)
SSW 55-5	5.7×10^{13}	2.4	1.7×10^{15}	3.81	7.8×10^{16}	0.64
SSW55-6	6×10^{13}	2.5	5.5×10^{16}	1.80	1.4×10^{18}	0.60

As these results show, it was difficult to control the active layer doping with this procedure. Since there was no significant improvement in the notch doping level, this procedure has now been discontinued in favor of the conventional growth process with the wafer behind the doping inlet.

Two cathode notch structures were made with growth of the notch directly on an n^+ Sn-doped substrate. Table 3.5 shows the doping level and thickness of various layers as derived from the C-V data and cleave and stain. The object of these two growth experiments without the buffer layer was to check the effect, if any, of residual H_2S after n^+ layer growth on the background doping and subsequently on the active layer doping. However, no appreciable difference was observed in notch doping or the active doping of these two growths and those grown with an n^+ buffer layer.

Notch structures grown with the buffer-notch-active and contact layer sequence displayed one persistent problem. A gradient in the doping profile after the notch consistently occurred. The same conditions of a run (SSW53-5) in which a flat active layer doping was achieved, were duplicated but still yielded a gradient in the active layer. After numerous attempts at changing growth processes to eliminate this gradient, a reverse structure with a buffer-active-notch and contact layer sequence was grown. The doping profile of this wafer (SSW59-5) is shown in Figure 3.12. A slight ripple in the contact layer doping was observed but was considered less consequential than a ripple or a gradient in the active layer. This wafer with the reverse structure was submitted for device fabrication to study the effect of this structure on the RF performance of the device.

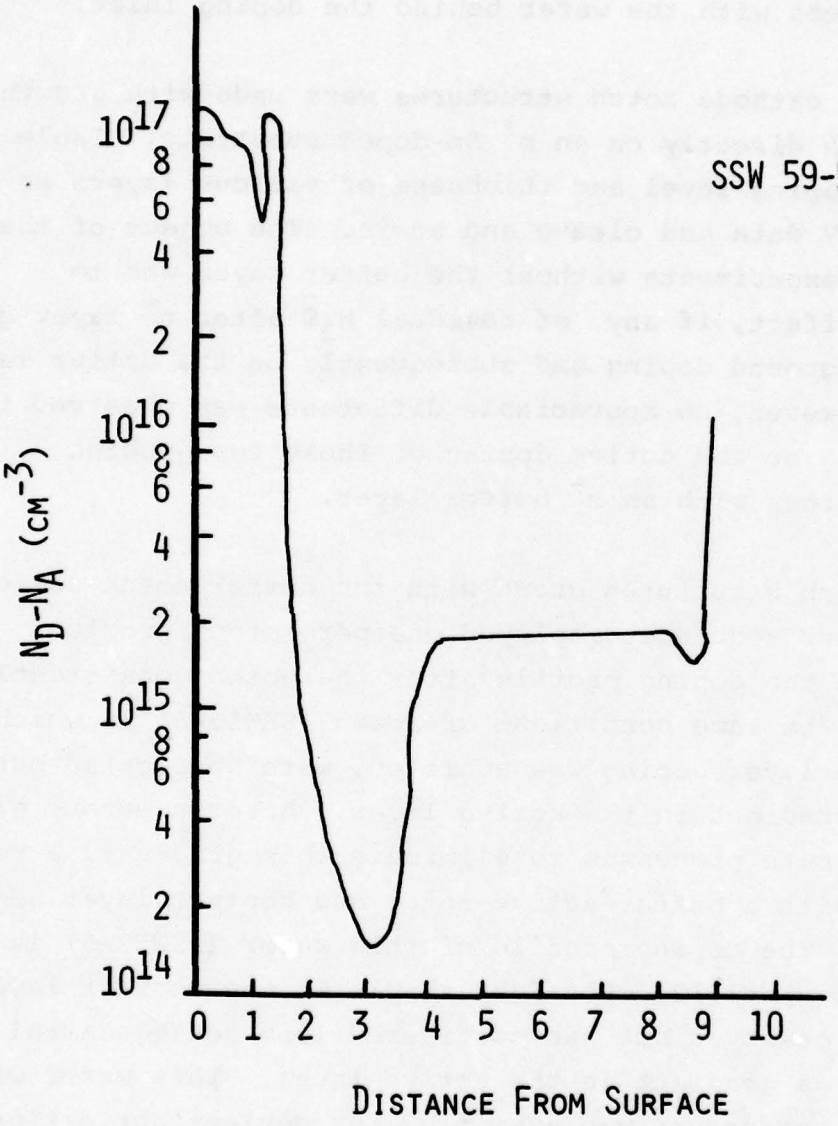


FIGURE 3.12. DOPING PROFILE OF REVERSE CATHODE NOTCH STRUCTURE

3.6 DISCUSSION OF GROWTH PROCESSES

$PC\ell_3$ mole fraction dependence of growth rate and carrier concentrations is very important for epitaxial layer control. The carrier concentration dependence on $PC\ell_3$ mole fraction is of particular importance in low doped growth such as notch layers of 10^{15} cm^{-3} or below. Figure 3.13 shows this dependence for material grown at Varian and RRE.

The effect of the high $PC\ell_3$ mole fraction can be seen in the 53 series runs. Runs 53-4 through 53-7 grown with a high mole fraction ($4x10^{-2}$) had notch doping levels of $3.1\text{-}6.2x10^{13}$ cm^{-3} whereas run 52-2 with a lower mole fraction ($9.23x10^{-3}$) had a much higher notch doping of $2.0x10^{14}$ cm^{-3}. Series 54 had very low notch doping as well except for 54-3 at $2.0x10^{14}$ cm^{-3}. However, 54-3 was a very narrow notch (1.0 μm) and would have been lower if it was as thick as the others.

Excellent quality of the growth layers with mirror smooth surfaces is being obtained by using InP substrates oriented 2^0 off (100) towards (110). These results have been obtained from two ingots. This allowed us to vary other VPE parameters over a wider range and still have good surface quality for device processing. Off orientation growth with the use of higher mole fraction $PC\ell_3$ has yielded consistently low background carrier concentrations allowing low doped notch profiles. An increase in background doping, however, has been observed after several contact layer and buffer layer growths. This is possibly caused as a cumulative effect of back diffusion of H_2S to the source and can conceivably be reduced by some kind of baffle arrangement. This factor is not severe enough at present to warrant immediate attention. Reproducibility of active layer doping level is, however, still poor, since the

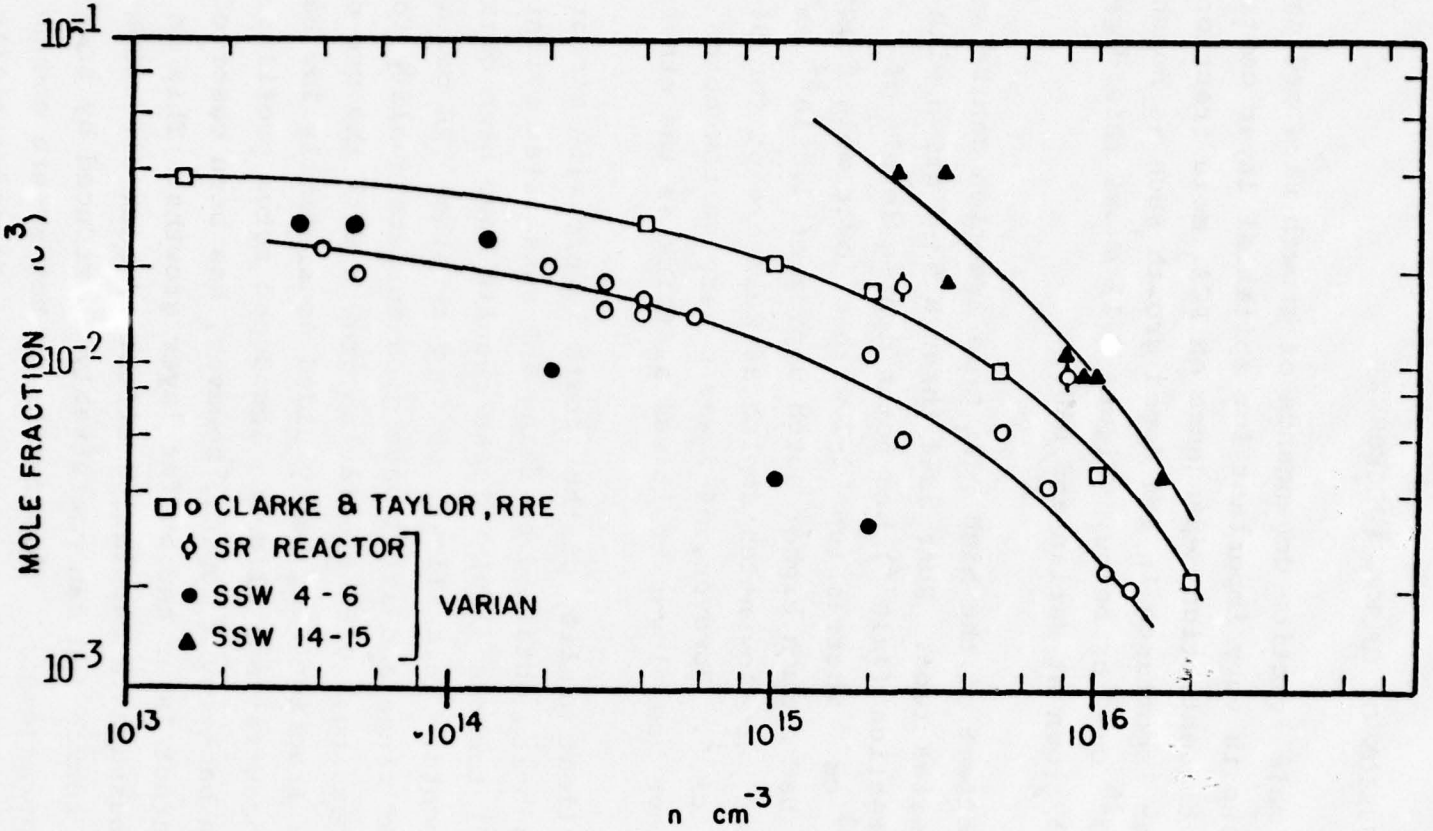


FIGURE 3.13. PCl_3 MOLAR FRACTION DEPENDENCE OF CARRIER CONCENTRATION

ppm of H_2S needed to attain the required doping level of $<1x10^{15}$ has been of the order of $<10^{-3}$.

The dependence of background doping level on In bakeout times has been studied. Two, sixteen and sixty-four hour bakeout times were used. The longer times produced higher mobilities, but increased silicon incorporation in the source from the boat and reactor walls resulted in higher doping levels. Short bakeouts and high $PC\ell_3$ mole fractions have been used to grow cathode notch material with the lowest notch doping levels yet measured. These results, combined with a significant improvement in growth rate control, allowed us to grow many cathode notch wafers suitable for device fabrication (see Table 3.3). Most of the notch doping levels were in the 10^{13} cm^{-3} range with a low of $3.1x10^{13}$ cm^{-3}. Doping profiles for four of these runs are shown in Figures 3.8 through 3.11. The notch profiles show very clean transitions for buffer/notch and notch/active layer interfaces as well as reasonably flat active layer profiles except for SSW53-7 (Figure 3.10) which drops rather sharply. Fairly flat active layer doping as low as $6x10^{14}$ cm^{-3} was obtained for wafer SSW53-5 (Figure 3.8).

It is interesting to note that run 52-9 had a low doped notch of $4.8x10^{13}$ cm^{-3}. It was grown with a high mole fraction but the indium source had a 16 hour bakeout compared to a 2 hour bakeout in series 53 and 54. However, it was also grown upstream of the H_2S doping inlet. This demonstrates the possible use of this growth technique if required in future runs to maintain or lower notch doping levels.

An important question is whether the low doping obtained with short 2 hour indium bakeout times is due to high purity

material or compensated material. Table 3.6 gives Hall and C-V data for mobility evaluation runs in series 52-54. Both series 52 and 54 with 16 hour and 2 hour bakeout times show normal high purity results. Series 54 also gave high purity results for both high and low $PC\ell_3$ mole fractions. Series 53 behaved differently and sample 53-1 showed carrier concentration freeze-out from room temperature to 77°K as well as low mobility data indicating compensation. By run 53-8, freeze-out did not occur but mobility remained low. Both of these runs used a low $PC\ell_3$ mole fraction (9.08×10^{-3}). However, most of the device runs in series 53 were grown with a high $PC\ell_3$ mole fraction (see Table 3.3) and run 53-9 gave good high purity mobility without carrier freeze-out when the high mole fraction was used. Device performance from these wafers is also consistent with high purity material and stable doping profiles.

The excessive wall deposits which interfere with maintenance of a constant growth rate were considerably reduced by going to a slightly sloping temperature gradient in the deposition zone. As a result, growth rates increased from a typical value of .07 μm/min. to 0.14 μm/min. At temperatures higher than 650°C, toward the upstream side, growth rates as high as 0.32 μm/min were obtained. Reduction in the wall deposits also improved the run to run reproducibility of the growth rates.

Table 3.7 gives growth rate data from three run series with the old profile. Standard deviations range from ±20% to ± 47.5% with an average of ± 35.3%. As shown in Table 3.8, standard deviations range from 4.1% to 7.9% (average ± 5.8%) with the new profile. In addition, the average growth rate is 2.2 times greater with the new profile. Growth rates

TABLE 3.6
VPE InP HALL SAMPLES, C-V DATA

RUN NO.	In BAKEOUT (hours)	PCl_3 MOLE FRACTION	C-V, 77°K (N_D-N_A) cm^{-3}	HALL DATA N_D-N_A cm^{-3} Room Temp	HALL DATA N_D-N_A cm^{-3} 77°K	HALL DATA μ_H, cm^2/v-sec Room Temp	HALL DATA μ_H, cm^2/v-sec 77°K
52-1	16	9.08×10^{-3}	7.6e14	1.2e15	1.1e15	4460	57,430
53-1	2	9.08×10^{-3}	4.2e15	1.5e16	4.5e15	2330	18,870
53-8	2	9.08×10^{-3}	5.4e15	9.0e15	7.6e15	2857	18,267
53-9	2	3.81×10^{-2}	3.1e15	3.7e15	3.1e15	3966	27,496
54-1	2	9.08×10^{-3}	1.4e15	5.7e14	4.8e14	4262	40,768
54-2	2	3.74×10^{-2}	1.2e15	1.6e15	1.3e15	4458	47,799

TABLE 3.7

VPE InP GROWTH RATES* - OLD FURNACE PROFILE

RUN NO.	EPI LAYER GROWTH RATE (μm/min)		
	NOTCH AND ACTIVE	ACTIVE	BUFFER
48-1	.059		.101
48-2	.042		.066
48-3	.072		.123
48-4	.035		.063
48-5	.027		.034
AVE	.047		.077
σ	± .018 (± 38.3%)		± .035 (± 45.5%)
49-4		.065	.101
49-5		.041	.055
49-6		.049	.078
49-7		.046	.071
AVE		.050	.076
σ		± .010 (± 20.0%)	± .019 (± 25.0%)
50-1			.086
50-2			.071
50-4			.127
50-5			.036
AVE			.080
σ			± .038 (± 47.5%)

* PCl_3 mole fraction was 9.23×10^{-3} during notch growth
Ratio of (buffer/notch and active) growth rate = 1.59

TABLE 3.8

VPE InP GROWTH RATES* - NEW FURNACE PROFILE

SSW RUN NO.	EPI LAYER GROWTH RATE (μm/min)	
	NOTCH AND ACTIVE	BUFFER
53-3	.135	.160
53-4	.134	.163
53-5	.137	.165
53-6	.148	.180
53-7	.141	.157
AVE	.139	.165
σ	± .0057 (± 4.1%)	± .0089 (± 5.4%)
54-3	.121	.160
54-4	.140	.140
54-5	.123	.143
54-6	.136	.157
54-7	.125	.138
54-8	.136	.170
54-9	.129	.152
AVE	.130	.151
σ	± .0074 (± 5.7%)	± .012 (± 7.9%)

* PCl_3 mole fraction was 4.0×10^{-2} during notch growth

Ratio of (buffer/notch and active) growth rate = 1.18

are given separately for buffer layers and either active or notch plus active layers. This is done because the growth rate is faster for initial growth when InP wall deposits are small. As a run progresses, wall deposits build up and the growth rate on the wafer slows down because more deposition occurs on wall deposits. It is of interest that the average ratios of the buffer to active/notch growth rate is only 1.18 for the new profile whereas it is 1.59 for the old profile. The new profile significantly reduces wall deposits and hence gives a more uniform growth rate for the entire epitaxial structure.

4. DEVICE FABRICATION

4.1 SCRIBE AND CLEAVE PROCESS

During this program, two processes were employed for the fabrication of InP devices; a) scribe and cleave process; and, b) integral heat sink (IHS) process. The scribe and cleave process, outlined in Figure 4.1, was used extensively during the early stages of this program while a high yield IHS process was being developed. The principal advantage of this fabrication process is the low thermal resistance which can be achieved. There are numerous disadvantages. The InP chip is susceptible to damage during the scribing, cleaving and ultrasonic bonding steps. The thermal resistance of package diode varies from diode to diode depending on the quality of the bond between the epitaxial layer metallization and the package. The minimum chip size allowed in the ultrasonic bonding step is still too large in area to be operated CW. Considerable in-package etching is required to adjust the device area for the desired operating current. Extensive in-package etching can lead to failure problems.

4.2 INTEGRAL HEAT SINK PROCESS

An integral heat sink (IHS) process has been developed for the fabrication of millimeter wave InP Gunn devices. In this IHS process, discrete gold heat sinks are plated up onto the epitaxial side of the wafer. Individual device mesas are formed by chemical etching from the substrate side. These IHS chips are then soldered into the device package.

1. THIN WAFER,
2. METALLIZE EPI AND SUBSTRATE SURFACES WITH Au-Ge/Ni/Au.
3. ALLOY CONTACTS.
4. Au ELECTROPLATE.
5. ETCH GRID PATTERN ON EPI SIDE THROUGH ACTIVE LAYER.
6. ETCH GRID PATTERN THROUGH SUBSTRATE METALLIZATION.
7. SCRIBE AND CLEAVE WAFER ALONG GRID PATTERN.
8. ULTRASONICALLY BOND DEVICE TO PACKAGE.
9. ATTACH LEADS.
10. IN PACKAGE ETCH TO DESIRED OPERATING CURRENT.

FIGURE 4.1. FABRICATION TECHNIQUE USING CLEAVING AND ULTRASONIC BONDING

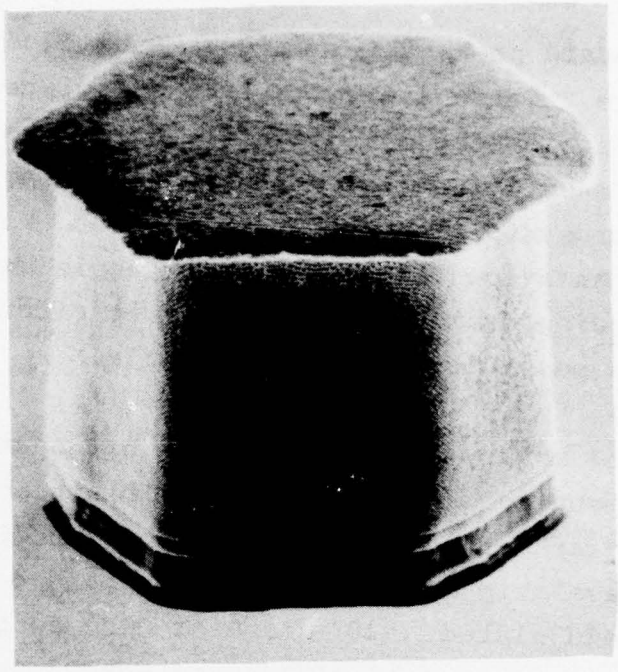
An IHS process has several important advantages over the scribe and cleave process. The wafer is not reduced to chips by a mechanical process, but rather by a controlled etching process, resulting in a more damage free chip. Since the gold heat sink is plated onto the epi layer metallization, it is in intimate contact with the device. Small surface irregularities do not destroy the thermal contact. The result is a much more reproducible thermal resistance from device to device. Since the device is soldered into the package as opposed to using ultrasonic bonding, it incurs less damage and a smaller device area can be used, reducing the amount of in-package etching which is required.

The IHS Process for InP which has been developed at Varian is outlined in Figure 4.2. It is a rather simple process, similar to that used on GaAs Gunn devices. It requires only three photographic exposures. It uses an $FEC\ell_3$ photosensitive etching technique to form the mesas.[9] Illuminated regions etch at a faster rate than unilluminated regions. The substrate contact pad is used as a shadow mask while the wafer is illuminated with collimated light. The result is a mesa whose cross sectional area very closely approximates that of the contact pad. Figure 4.3 is an SEM photo illustrating a typical mesa formed using this procedure from cathode notch wafer EE156. The mesa walls are very steep and the contact undercutting is small compared to that which is achieved using an isotropic etch.

This process is useable with substrates of almost any thickness. Devices are routinely made from wafers ranging in thickness from 20 μm to 50 μm. The final device area is not determined by the mask size and substrate thickness but principally by the shadow mask dimensions. Device geometries

1. THIN WAFER TO 50 um
2. SPUTTER Au-Ge/Ni/Au ON BOTH EPI AND SUBSTRATE SURFACES - ALLOY
3. DEFINE HEAT SINK AREAS
4. PLATE UP Au HEAT SINKS
5. BACKSIDE ALIGNMENT OF SUBSTRATE CONTACT WITH HEAT SINKS
6. MASK AND ETCH SUBSTRATE CONTACT METALLIZATION
7. ETCH MESAS $FeCl_3$ PLUS ILLUMINATION
8. SOLDER INDIVIDUAL DEVICES INTO PACKAGE.
9. ATTACH LEADS
10. IF NECESSARY, IN-PACKAGE ETCH TO DESIRED OPERATING CURRENT

FIGURE 4.2. FABRICATION SEQUENCE FOR InP IHS DEVICES



1.25x800

FIGURE 4.3. SEM PHOTO OF InP IHS MESA FABRICATED FROM CATHODE NOTCH WAFER EE156

other than circular mesas, e.g. ring structures, have been fabricated by this process.

4.3 PEDESTAL MOUNTED DIODES

The standard package for mm-wave Gunn diodes has been the N-34 package. There are parasitics associated with this package which become more significant at the higher frequencies. In addition, the N-34 package is not an optimum package for microstrip applications. For such applications, a package which has a low thermal resistance, is replaceable, and is capable of being mounted in a microstrip circuit with as little labor as possible would be desirable.

Some preliminary development work has been completed on a pedestal mounted diode for microstrip applications. Figure 4.4 is a photograph of an InP pedestal mounted diode. A scribe and cleave chip was ultrasonically bonded onto a polished and gold plated .010" diameter OFHC copper pedestal which is .050" long. A gold ribbon was bonded to the top contact of the diode. A resin was carefully applied to the area around the bond to provide mechanical support. This pedestal mounted diode can be inserted through a .010" diameter hole in a microstrip circuit, and the pedestal either clamped or soldered into place. The bond wires can then be bent into place and bonded or silver epoxied to the appropriate point in the microstrip circuit.

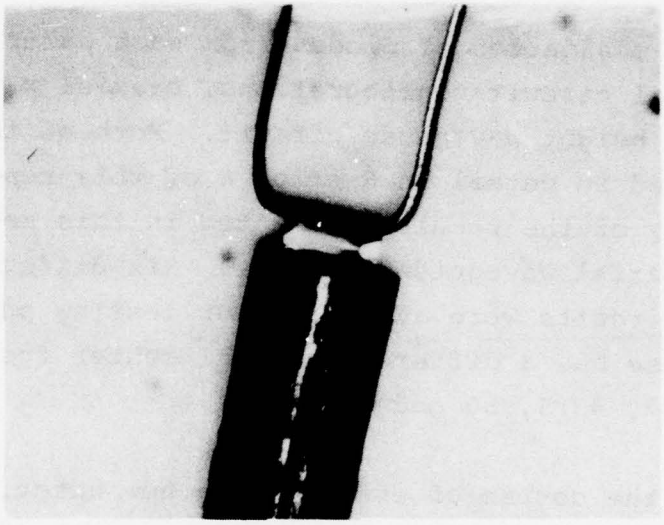


FIGURE 4.4. PEDESTAL MOUNTED InP GUNN DEVICE FOR MICROSTRIP APPLICATION

5. RF EVALUATION OF WAFERS

5.1 EVALUATION OF RF PERFORMANCE

This section summarizes the rf performance of all of the different wafers evaluated during this program. Three layer wafers and cathode notch wafers are compared. The dependence of noise measure on the active layer $n\ell$ product is discussed. In addition, the effects and limitations of the various doping parameters on the gain, noise figure and bandwidth are discussed.

The evaluation of diodes from each wafer was performed in two principal circuit configurations, coaxial waveguide circuit and reduced height waveguide circuit. Both of these circuits are discussed in detail in Section 6 of this report. However, the majority of the results presented in this section were obtained with the coaxial waveguide circuits. Six different coaxial waveguide circuits were available for testing purposes. Each of these has a different nominal center frequency, 29.5, 33, 37, 43.5, 50 and 56.5 GHz.

In the course of evaluating a new wafer, a number of diodes from this wafer were tested in several of the test circuits to determine the optimum frequency range of operation. In Ka-band and the 40-60 GHz band, reflectometer gain measurements were often made to eliminate bandwidth and ripple limitations introduced by circulators. Once the optimum frequency range was determined, a circulator coupled amplifier configuration was used to make gain and noise figure measurements. Noise measures were then calculated. Diodes having different cross sectional areas were evaluated from each

new wafer, as there was an optimum diode area for highest gain in a certain frequency range. In addition, bias conditions were varied to determine optimum bias voltage for maximum gain and/or minimum noise figure. In general, circuit parameters were adjusted to give a wide band gain response for this evaluation process. From these measurements two figures of merit, noise measure and the gain$^{1/2}$ bandwidth product, were derived which allow a relative comparison of the performance of the different wafers.

5.2 TEST CIRCUITS FOR MEASUREMENT OF GAIN AND NOISE FIGURE

The Ka-band test circuit used to perform gain and noise figure measurements is shown in Figure 5.1. The manual waveguide switch is shown in the position for making noise figure measurements. The noise source which was used was an AIL noise tube having an ENR of 16.3 dB, and the mixer was a Spacekom mixer FKa-U. The noise power was measured at an I.F. of 60 MHz. Noise figure measurements were made using both the manual and automatic Y factor methods. Agreement between both methods was good. Determination of the noise figure of the InP amplifier under test over a wide frequency range by the automatic method required accurate measurement versus frequency of the loss of the circuit between the noise tube and the amplifier under test, the gain of the amplifier, the loss of the circuit between the amplifier and the mixer, and the noise figure of the mixer. The manual Y factor method required accurate measurement versus frequency of the loss of the circuit between the noise tube and the amplifier under test, as well as accurate calibration of the microwave attenuator being used. Because the gain of the InP amplifier under test at certain frequencies of interest was as low as 3 dB, the correction factors due to circuit losses

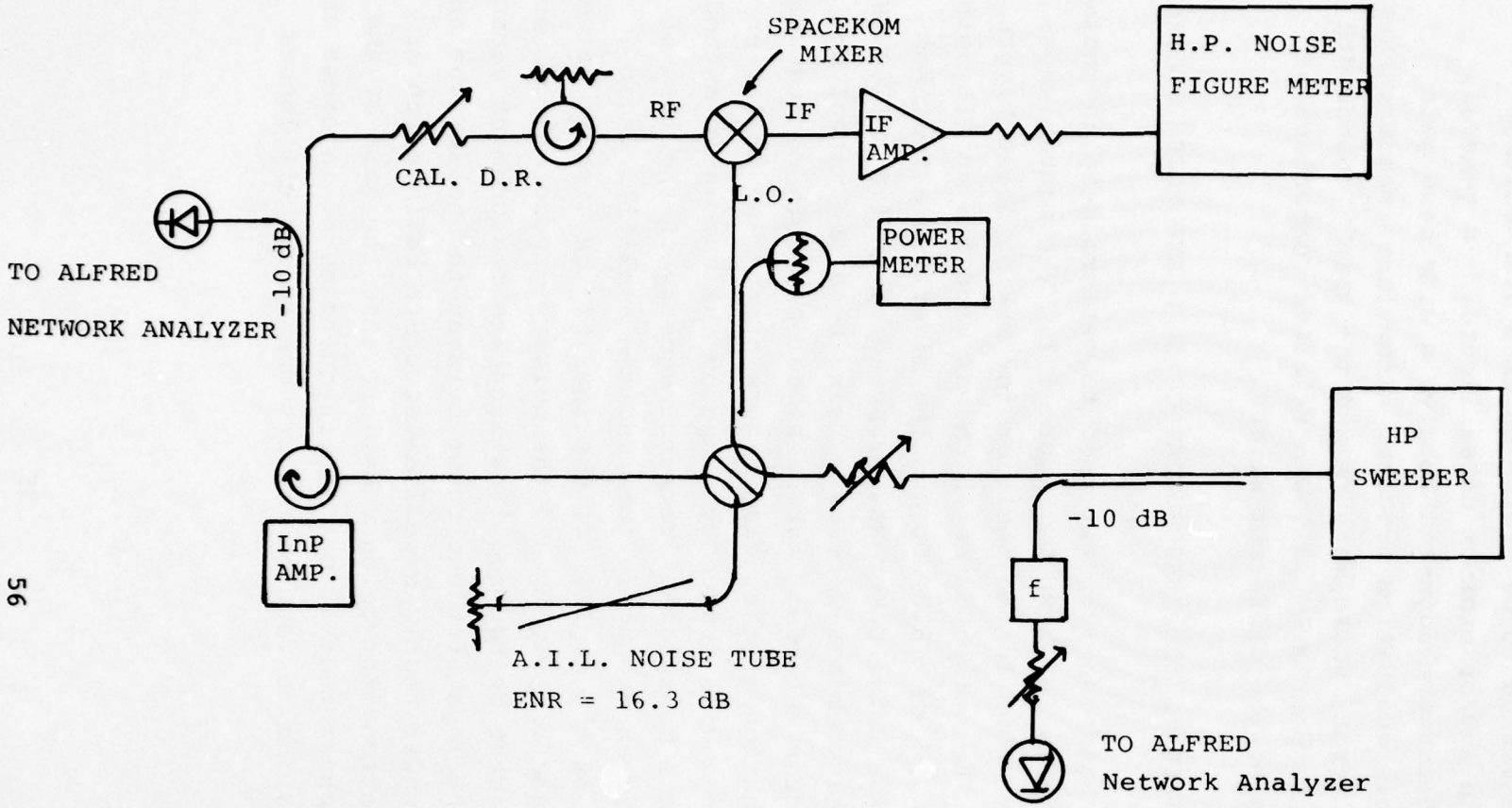


FIGURE 5.1 KA-BAND GAIN AND NOISE FIGURE MEASUREMENT CIRCUIT

and mixer noise figure are significant and must be computed. The manual Y factor method required less correction factors, and as a result was simpler and more accurate for making measurements over a wide range of frequencies and amplifier gain levels. The values of noise figure reported in this section for Ka-band were obtained using the manual Y factor method, and have been corrected for circuit and circulator losses.

The circuit used to perform gain and noise figure measurements in the 40-60 GHz band is shown in Figure 5.2. A Micro-Now sweeper was used in obtaining gain measurements, but the BWO was found to be too noisy to use as an L.O. for the Spacekom mixer in making noise figure measurements. Instead a mechanically tuned Gunn oscillator was used as an L.O. A C.P. Clare noise tube having an ENR of 15.4 dB was used as a noise source and the noise power was measured at an I.F. of 60 MHz. Noise figure measurements are made using the manual Y factor method. Note that the noise figures reported here for the 40-60 GHz band have not been corrected for circuit and circulator losses as they were in Ka-band.

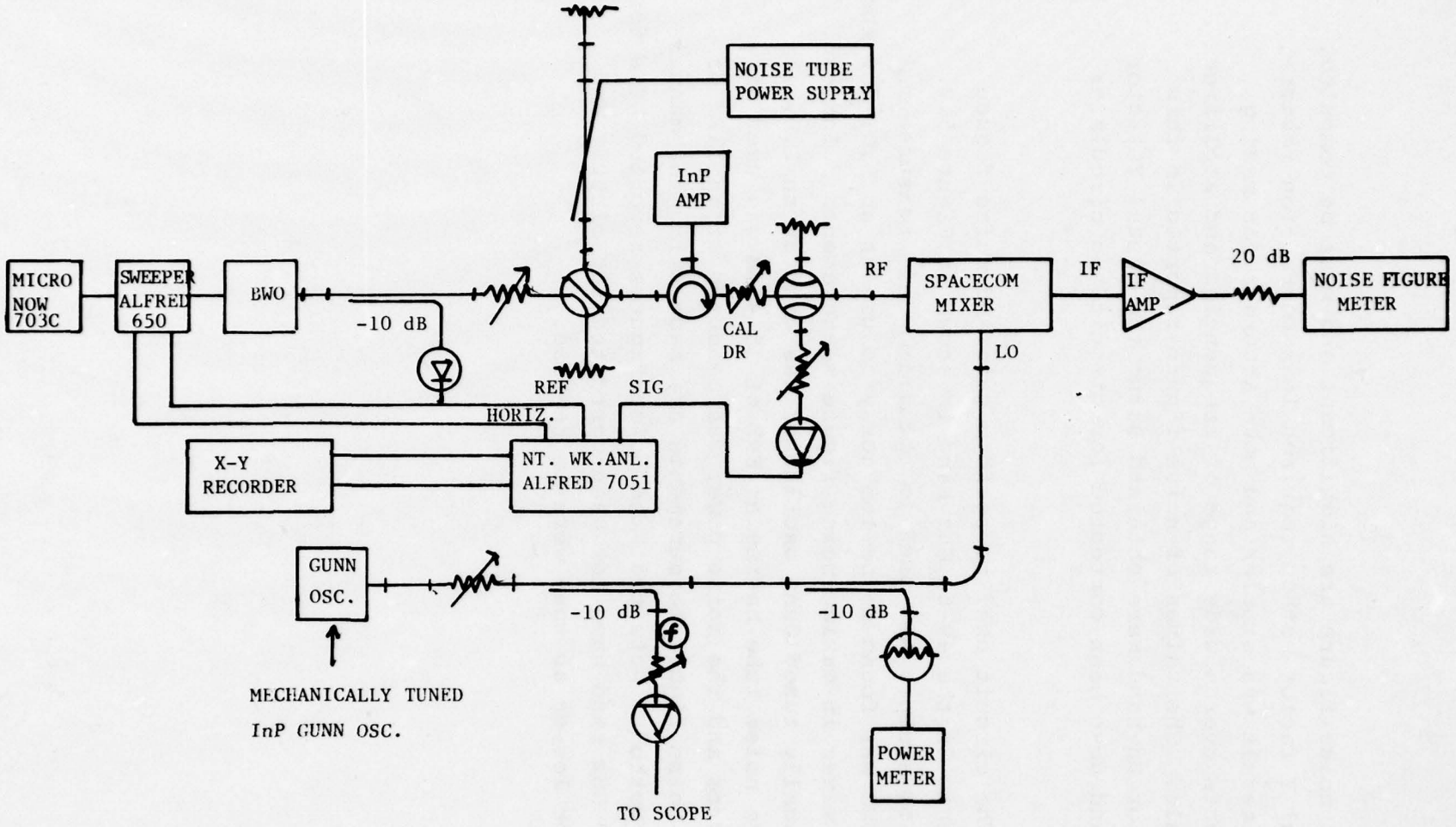


FIGURE 5.2 40-60 GHz GAIN AND NOISE FIGURE MEASUREMENT CIRCUIT

5.3 THREE LAYER WAFERS

Although the main emphasis of this program was the development of cathode notch InP devices, a small number of three layer wafers were grown in the early stages of this program. These devices were used primarily for circuit development purposes while cathode notch growth techniques were being developed. Figure 5.3 summarizes the active layer length and doping of the three layer wafers whose rf performance was evaluated. Horizontal bars are used for several of the wafers because the active layer doping displayed a gradient. The length of the bar indicated the variation in doping with thickness and not variation in doping at different points across the wafer. Table 5.1 summarizes the doping profile parameters and the rf performance of each three layer wafer. The maximum and minimum gain and noise figure, measured in a specific frequency interval, are listed. The minimum noise measure is also tabulated. Typical $gain^{1/2}$-bandwidth products for each wafer are also listed. To calculate this product the peak gain and the full 3 dB bandwidth were used. The $gain^{1/2}$ bandwidth product depends not only on the device but also on the test circuit which is being used. It is a figure of merit of the device circuit combination. Wafer EE98 yielded the best wide band low noise amplification. The lowest noise measure of 10.0 dB was obtained from EEE97 but the gain response was very narrowband.

In Figure 5.4, the noise measures of these three layer wafers are plotted against their $n\ell$ products. Also plotted are the theoretically predicted noise measures of a uniform field device. As expected, the noise measure decreases with $n\ell$ product down to approximately 4×10^{11} cm^{-2}. The average field levels in these devices ranged from 20 to 30 kv/cm. Thus, these noise measures are slightly higher than those predicted for a uniform

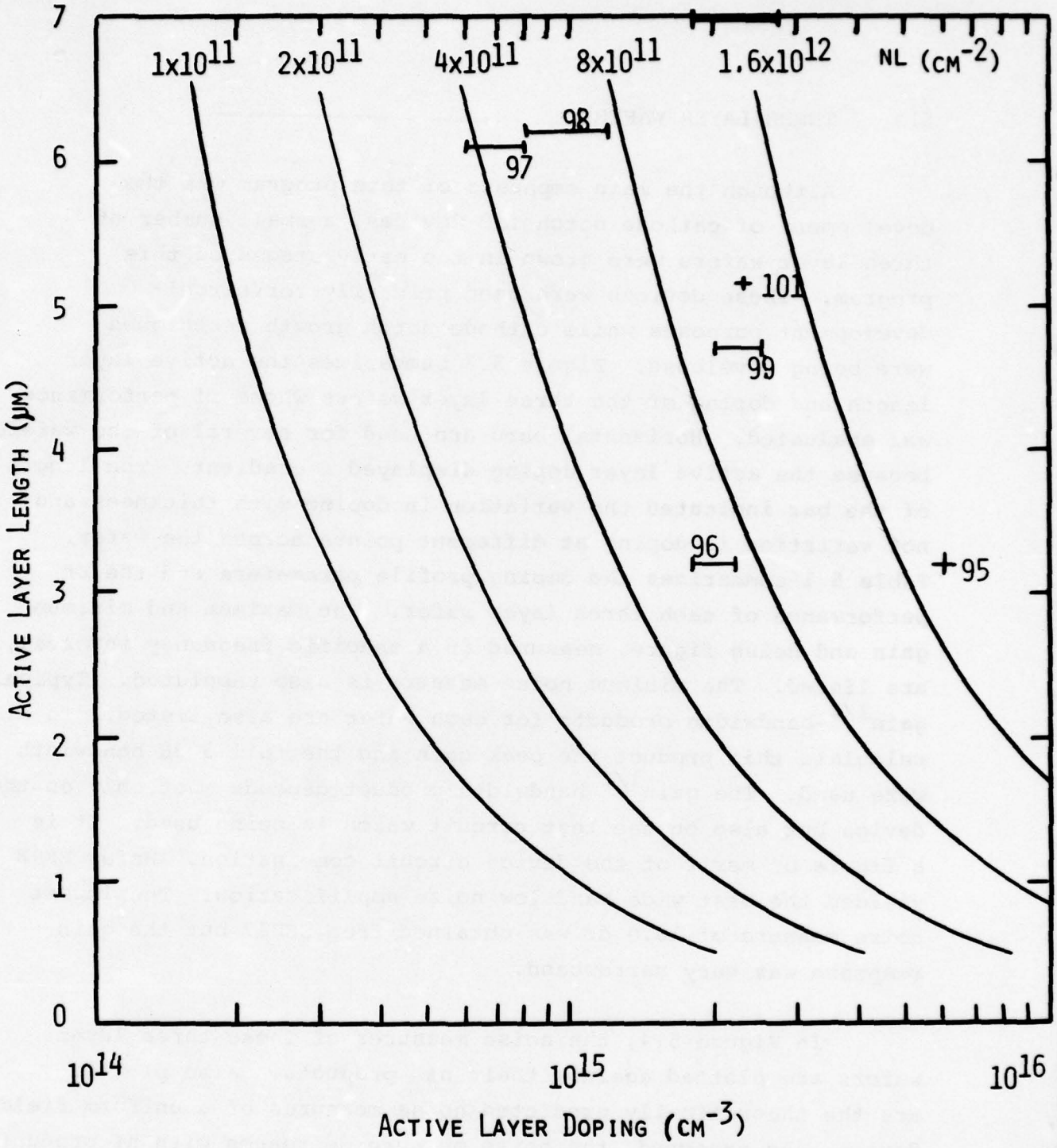


FIGURE 5.3. SUMMARY OF ACTIVE LAYER LENGTH AND DOPING OF THREE InP WAFERS

TABLE 5.1 DOPING PROFILE PARAMETERS AND RF PERFORMANCE OF THREE LAYER WAFERS

		ACTIVE LAYER		RF PERFORMANCE						
WAFER	VPE RUN	n (cm^{-3})	ℓ (μm)	FREQUENCY (GHz)	GAIN (dB) MAX	GAIN (dB) MIN	NOISE FIGURE (dB) MAX	NOISE FIGURE (dB) MIN	NOISE MEASURE (dB)	$GAIN^{1/2}$ x BANDWIDTH (GHz)
EE95	44-4	6.0×10^{15}	3.2	34.3-38.3	---	---	---	---	---	10.6
				40.2-46.2	8.0	5.0	---	---	---	15.1
EE96	44-5	$1.8\text{-}2.0 \times 10^{15}$	3.2	43.8-47.1	10.0	7.0	14.5	13.6	14.6	10.4
EE97	46-12	$0.6\text{-}0.8 \times 10^{15}$	6.1	33.0-38.8	5.5	2.5	---	----	---	10.9
				29.7-30.9	7.5	4.5	10.0	---	10.4	3.8
EE98	47-4	$0.8\text{-}1.2 \times 10^{15}$	6.2	29.8-35.7	8.5	5.5	11.2	---	11.5	15.7
EE99	47-3	2.0-2.5	7.7	27-34	9.0	6.0	---	---	---	19.7
				34.5-35.7	10.0	7.0	12.9	---	13.1	3.8
EE101	47-7	2.3×10^{15}	5.1	27.2-33.5	8.0	5.0	15.2	12.9	14.6	15.8
EE107	49-6	$1.8\text{-}2.7 \times 10^{15}$	7.0	30.2-36.1	6.0	3.0	13.6	---	14.7	11.8

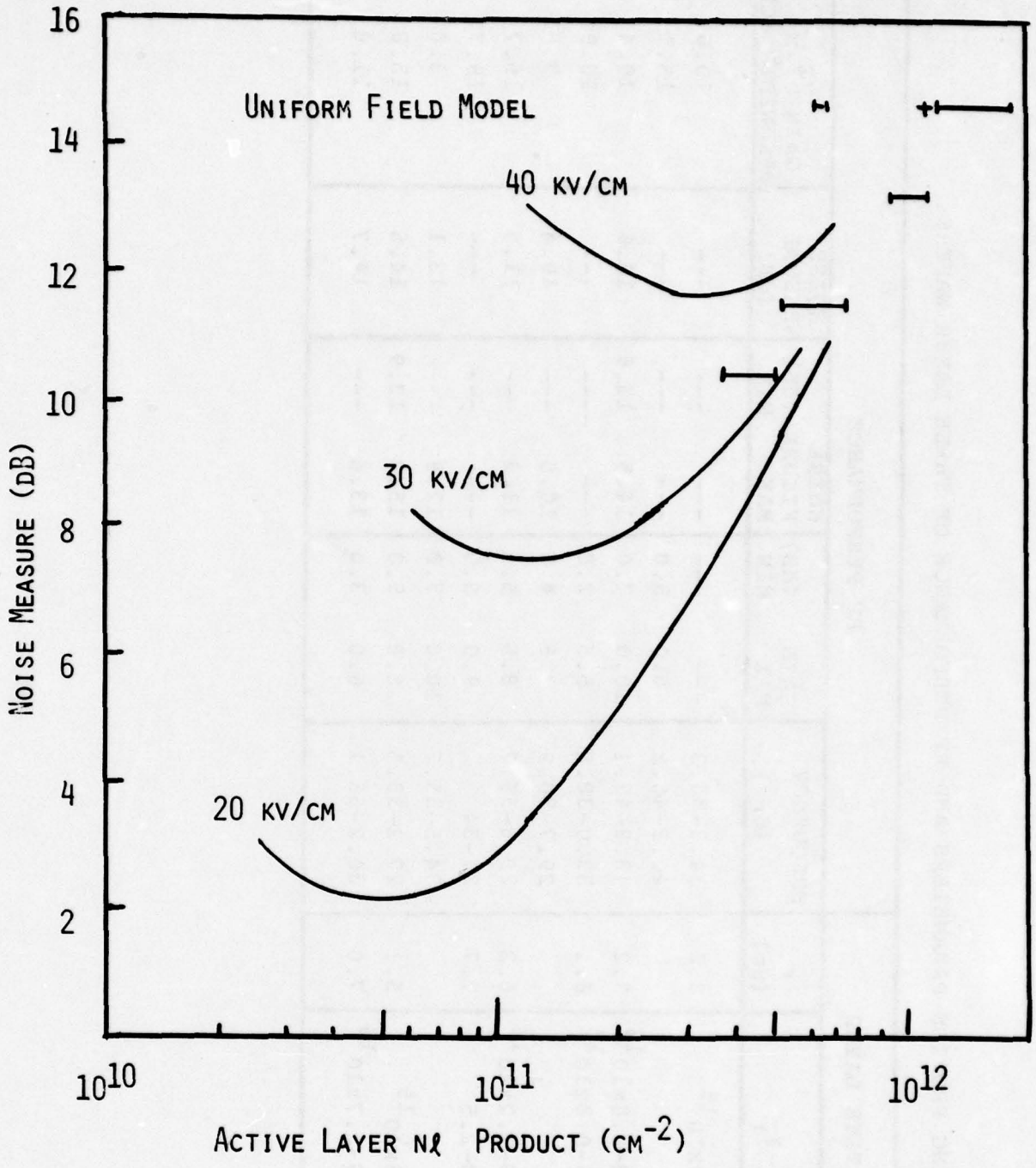


FIGURE 5.4. NOISE MEASURE VERSUS ACTIVE LAYER NL PRODUCT FOR THREE LAYER WAFERS

field device. As mentioned in Section 2 of this report, at high $n\ell$ products, there is no appreciable difference in the noise measure of a three layer device and an ideal uniform field device. At $n\ell$ products less than 4×10^{11} cm^{-2} it is expected that noise measures of three layer devices will not decrease further with decreasing $n\ell$ product.

5.4 CATHODE NOTCH WAFERS

The majority of the InP wafers grown for this program were of the cathode notch structure. Figure 5.5 summarizes the active layer length and doping of all the wafers whose rf performance was evaluated. Most of the wafers exhibited a gradient in the active layer doping. The length of the horizontal bar for a given wafer indicates the variation in doping with thickness of the active layer. Wafers with $n\ell$ products ranging from 9×10^{10} to 1.2×10^{12} cm^{-2} were grown. The majority of the cathode notch wafers displayed significant gradients, which degraded their performance. In the operation of a low noise cathode notch device, the notch width and doping are as important as the active layer parameters. The noise measure is dependent on the notch parameters as well as the active layer parameters.

Table 5.2 lists the active layer and notch layer parameters as well as typical rf performance of each cathode notch wafer. Four wafers yielded low noise measures—EE120, EE121, EE122 and EE127. Active layer $n\ell$ products of these wafers ranged from 8×10^{10} cm^{-2} to 2.4×10^{11} cm^{-2}. The noise measures of all the cathode notch wafers are plotted in Figure 5.6 as a function of active layer $n\ell$ product. Noise measure is continuing to decrease with $n\ell$ product down to at least 9×10^{10}, where EE127 yielded a noise measure of 7.7 dB. Wafers with lower $n\ell$ products have correspondingly lower negative resistances, and tend to yield lower gain, smaller bandwidth. Improved circuit matching is required to achieve higher gain out of such low doped devices.

EE119 and EE130 are two wafers which yielded wideband gain with somewhat higher noise measures (11.6 dB and 9.6 dB, respectively). For the test circuits available these two wafers provided the best compromise of gain, bandwidth and noise for a practical amplifier. Devices from these two wafers were

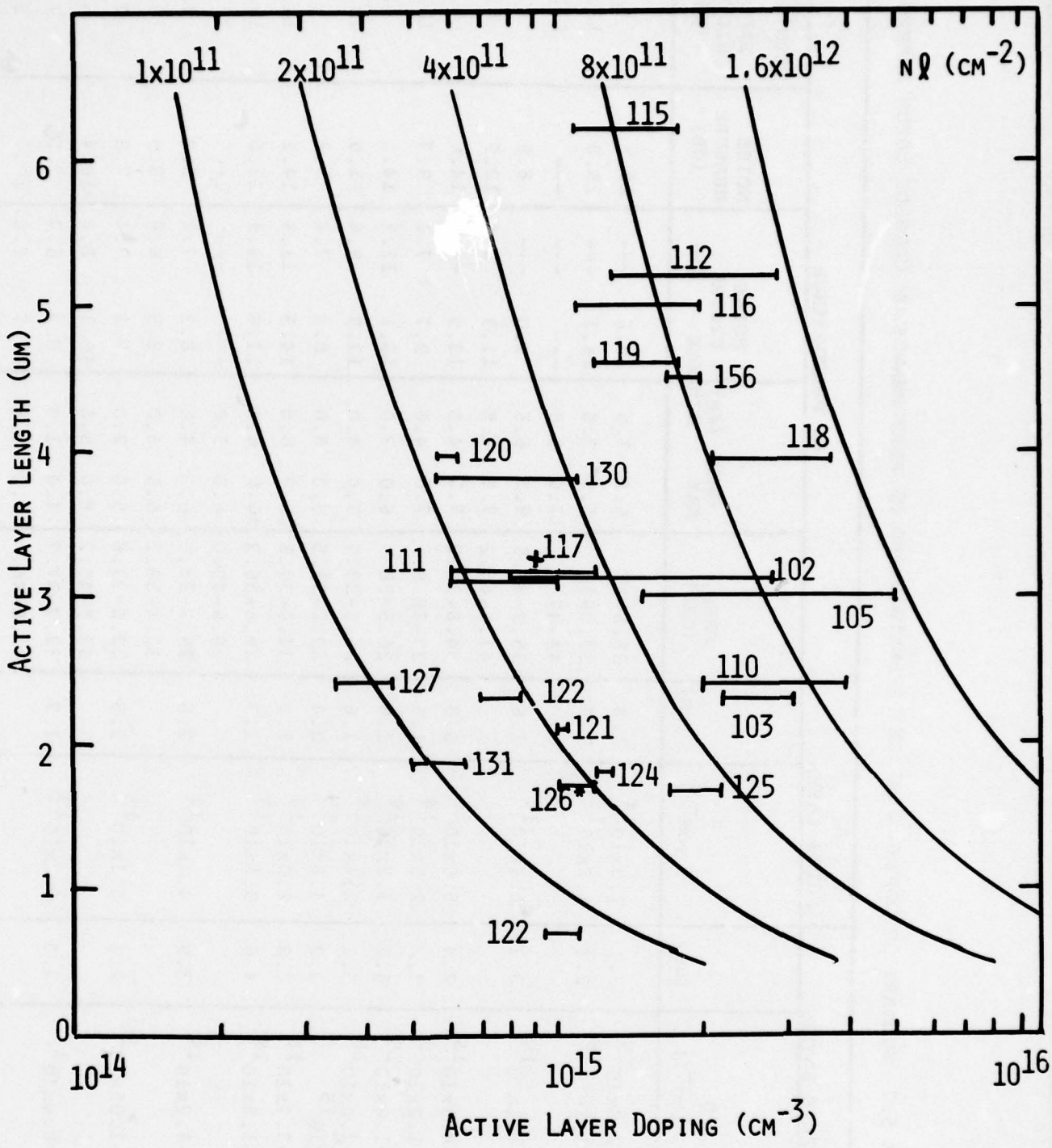


FIGURE 5.5 SUMMARY OF ACTIVE LAYER LENGTH AND DOPING OF CATHODE NOTCH InP WAFERS

TABLE 5.2 SUMMARY OF DOPING PROFILE PARAMETERS AND RF PERFORMANCE OF CATHODE NOTCH WAFERS

		ACTIVE LAYER		NOTCH LAYER		RF PERFORMANCE						
WAFER	VPE RUN	n (cm^{-3})	ℓ (μm)	n (cm^{-3})	ℓ (μm)	FREQ. (GHz)	GAIN (dB) MAX	GAIN (dB) MIN	NOISE FIGURE MAX	NOISE FIGURE MIN	NOISE MEASURE (dB)	$GAIN^{1/2}$ x BAND-WIDTH (GHz)
EE102	47-8	$0.8\text{-}2.8\times10^{15}$	3.1	7.0×10^{14}	1.4	33.5-37	6.5	3.5	15.6	---	16.5	7.4
EE103	47-9	$2.2\text{-}3.1\times10^{15}$	2.3	1.2×10^{15}	1.0	33.2-39	6.5	3.5	14.1	---	15.0	12.2
						44-47	12.0	9.0	---	---	---	11.9
EE104	48-1	$0.6\text{-}1.1\times10^{15}$	3.1	1.4×10^{14}	1.6	35.9-37.5	9.5	6.5	9.0	---	8.9	4.8
						41.5-45.2	7.5	4.5	11.9	8.4	12.5	8.8
EE110	48-4	$2.0\text{-}4.0\times10^{15}$	2.4	5.6×10^{14}	0.9	34.8-38.2	7.5	4.5	13.9	---	14.6	8.1
EE111	48-7	$0.6\text{-}1.2\times10^{15}$	3.2	2.5×10^{14}	1.3	33-38.2	7.0	4.0	9.7	7.1	9.7	10.7
EE115	51-2	$1.2\text{-}1.8\times10^{15}$	6.2	3.2×10^{14}	1.8	26.5-28	6.0	3.0	13.1	11.9	14.1	4.0
EE116	51-3	$1.1\text{-}2.0\times10^{15}$	5.0	2.4×10^{14}	1.6	26.5-33.5	7.0	4.0	12.5	9.6	11.0	15.0
EE117	52-9	0.9×10^{15}	3.2	4.8×10^{13}	2.4	29.2-31.5	5.0	3.0	8.3	7.4	9.2	5.7
EE118	53-2	$2.1\text{-}3.7\times10^{15}$	3.9	2.0×10^{14}	1.7	31.0-35.5	10.0	6.0	14.3	11.5	14.1	11.7
EE119	53-4	$1.2\text{-}1.8\times10^{15}$	4.6	5.1×10^{13}	1.7	29.6-36.2	10.0	6.0	11.8	11.1	11.6	19.0
						26.5-40.0	8.0	5.0	---	---	---	34.0
EE120	53-5	$5.6\text{-}6.2\times10^{14}$	3.9	3.2×10^{13}	2.5	29.8-34.0	6.5	4.0	8.3	7.1	8.2	9.3
						33.4-38.2	6.0	3.0	8.5	6.8	8.5	9.6
EE121	53-6	$1.0\text{-}1.05\times10^{15}$	2.1	3.1×10^{13}	2.8	32.6-37.8	5.0	2.0	7.2	7.1	7.8	9.2
						43.0-45.2	8.0	5.0	10.1	8.8	10.4	5.5
EE122	53-7	$7.0\text{-}8.4\times10^{14}$	2.3	6.2×10^{13}	1.7	32.7-37.7	4.0	1.0	8.3	6.7	7.5	7.9
						43.6-46.4	6.5	3.5	9.7	8.6	10.7	5.9

TABLE 5.2 (Cont.)

WAFER	VPE RUN	ACTIVE LAYER n (cm^{-3})	ACTIVE LAYER ℓ (μm)	NOTCH LAYER n (cm^{-3})	NOTCH LAYER ℓ (μm)	RF PERFORMANCE FREQ. (GHz)	GAIN (dB) MAX	GAIN (dB) MIN	NOISE FIGURE MAX	NOISE FIGURE MIN	NOISE MEASURE (GHz)	$GAIN^{1/2}$ x BAND WIDTH (GHz)
EE123	54-3	$.94\text{-}1.1\times10^{15}$	0.7	2.0×10^{14}	1.0	40-60	no gain		---	---	---	---
EE124	54-5	$1.2\text{-}1.3\times10^{15}$	1.8	5.6×10^{13}	1.8	43-44.5	9.5	6.0	10.1	8.6	9.9	4.8
EE125	54-7	$1.7\text{-}2.2\times10^{15}$	1.7	7.7×10^{13}	1.5	33.6-38.3	5.0	3.0	9.6	8.3	10.0	9.4
						40.8-46.1	7.0	4.0	10.3	9.8	10.8	10.6
EE126	54-8	$1.0\text{-}1.2\times10^{15}$	1.7	1.05×10^{14}	1.6	33-37.5	5.0	3.0	8.8	7.0	9.1	8.0
						41.8-45.8	6.0	3.0	9.8	7.6	10.4	8.0
EE127	54-9	$3.5\text{-}4.6\times10^{14}$	2.4	5.7×10^{13}	1.8	32-39	4.0	1.0	7.1	6.3	7.7	12.7
						42.3-44.8	6.0	3.0	8.8	6.9	9.4	5.0
EE130	55-5	$.66\text{-}1.1\times10^{15}$	3.8	5.7×10^{13}	2.4	33-38.8	7.0	4.0	9.7	8.3	9.6	13.0
EE131	55-6	$.5\text{-}.64\times10^{15}$	1.9	6.0×10^{13}	2.5	33-38.3	3.0	2.0	7.1	5.8	8.0	7.5
EE156	59-5	$1.7\text{-}2.0\times10^{15}$	4.5	1.5×10^{14}	2.5	35-40	11.0	8.0	13.0	11.4	11.8	17.7

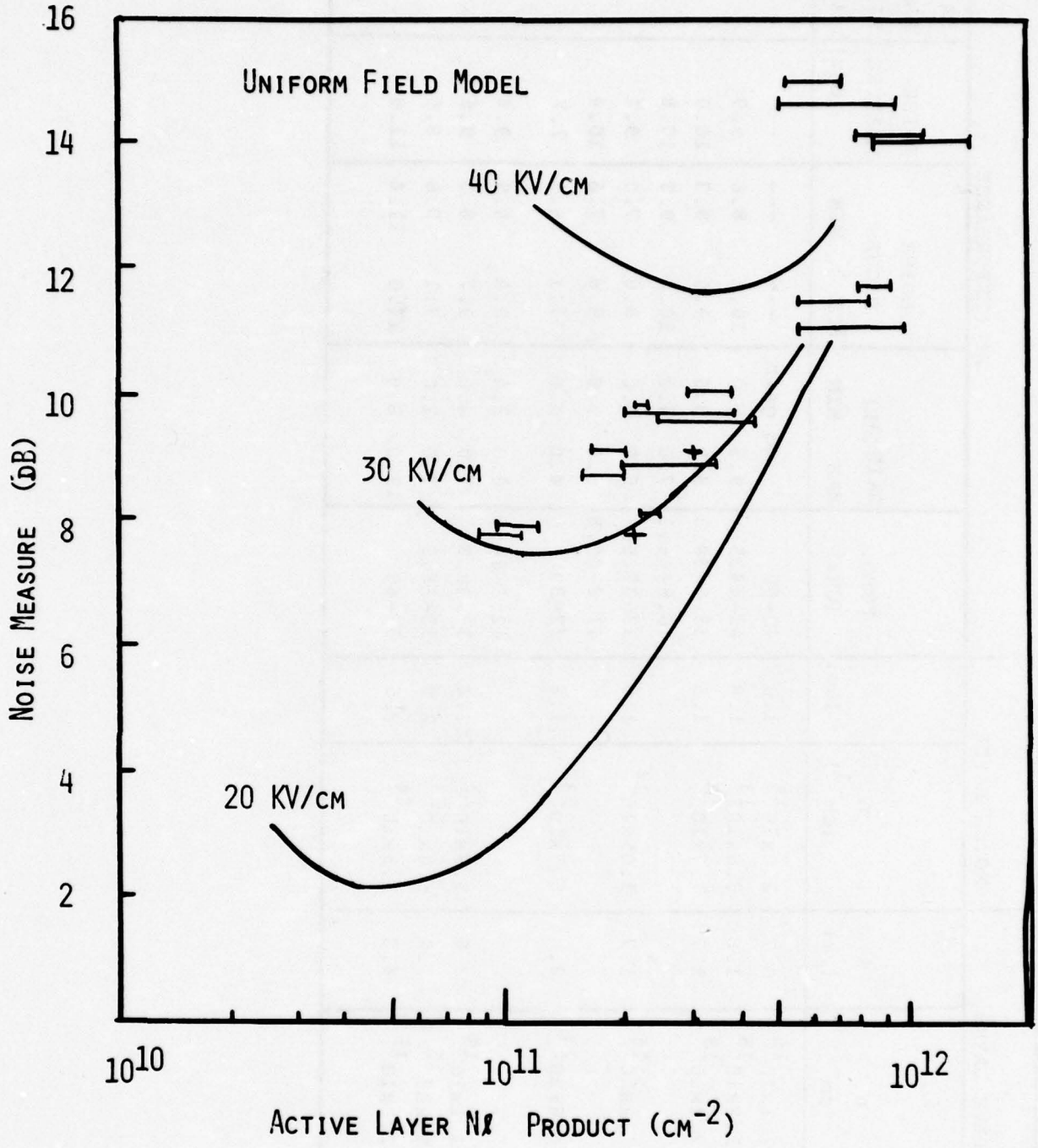


FIGURE 5.6 NOISE MEASURE VERSUS ACTIVE LAYER NL PRODUCT FOR CATHODE NOTCH WAFERS

used in the final Ka-band amplifier. With proper circuit matching devices from these wafers can provide very wideband gain. As shown in Section 6.3 of this report, a single device from EE119 provided a gain response over the entire frequency range from 26.5-40 GHz.

For a uniform field device a bias field of twice the threshold field (10 KV/cm) yields the lowest noise measure. For bias voltages which yielded fields of 20-25 KV/cm, noise measures of the cathode notch devices were slightly higher than expected for a uniform field device. There are two possible explanations. First, very few notch devices had flat active layer doping profiles and at the same time the proper notch width and depth. Second, for low doped active layers, the n^- notch width becomes comparable to or greater than the active layer thickness. Thus, the voltage drop across the notch layer becomes significant, effectively adding a positive series resistance to the device. This latter problem could be solved by the use of p-type notch.

6. CIRCUIT DEVELOPMENT

Throughout this program, the emphasis of the circuit development effort was low noise, wide band amplification. To achieve low noise operation, a low doped cathode notch InP device must be used. The lower negative resistance of such devices requires optimum matching of the circuit and device to achieve wide band response. This section discusses small signal impedance measurements performed on Ka-Band InP devices and amplifier circuits. Two types of circuits were investigated; a coaxial-waveguide circuit and a reduced height waveguide circuit. Full band gain response was achieved with the reduced height circuit. This section also discusses the performance of circulators which are an integral part of a reflection amplifier.

6.1 DEVICE CHARACTERIZATION AND MODELING

Small signal impedance measurements were performed on InP devices in Ka-band using a Hewlett-Packard network analyzer equipped with an R8747A transmission reflection test set. A direct measurement of the impedance of a packaged InP diode is not possible at these frequencies. However, using standard de-embedding techniques,[10] a diode's impedance can be derived.

To perform impedance measurements on diodes they were mounted in the coaxial-waveguide circuit shown schematically in Figure 6.1. The impedance of the circuit, Z_A, presented to the diode and the impedance of the diode, Z_B, presented to the circuit at plane DD' were determined from measurements made at the input plane CC' using de-embedding techniques. The measurement of three reflection coefficients at the input plane CC' for three known load impedances at the output plane

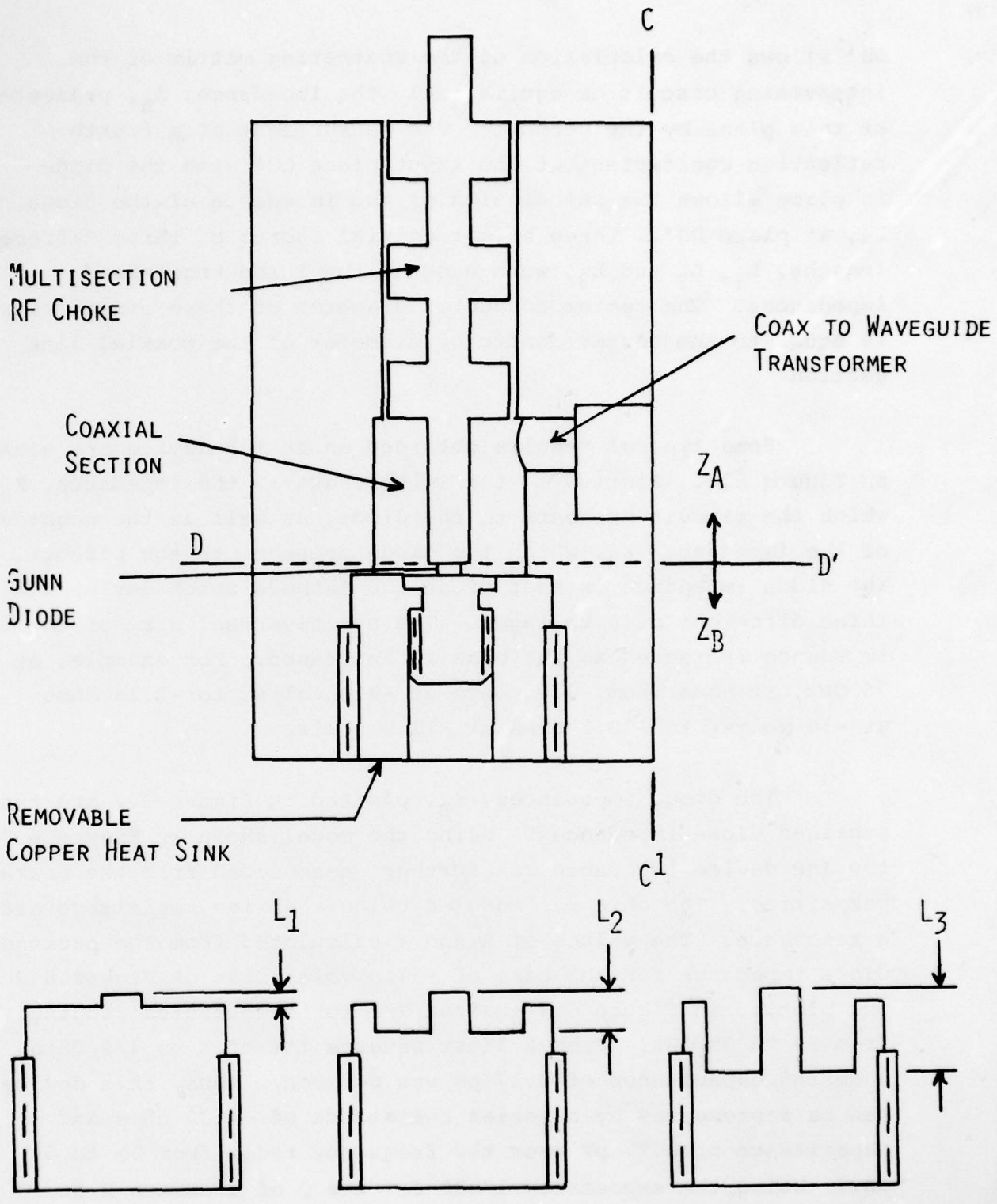


FIGURE 6.1 COAXIAL-WAVEGUIDE CIRCUIT AND THREE KNOWN LOAD IMPEDANCES USED FOR DE-EMBEDDING

DD' allows the calculation of the scattering matrix of the intervening circuit or equivalently the impedance, Z_A, presented at this plane by the circuit. The measurement of a fourth reflection coefficient at the input plane CC' with the diode in place allows the calculation of the impedance of the diode, Z_B, at plane DD'. Three offset coaxial shorts of three different lengths, L_1, L_2 and L_3, were used as the three known load impedances. The center conductor diameter of these offset shorts is equal to the center conductor diameter of the coaxial line section.

Some typical results obtained on an InP device are shown in Figure 6.2. Plotted on the Smith chart is the impedance, Z_A, which the circuit presents to the diode, as well as the negative of the impedance, Z_B, which the diode presents to the circuit. The diode impedance is that of an InP cathode notch device for three different bias voltages. The negative real part of the diode impedance increases as the bias is increased. For example, at 35 GHz, it goes from -3.95 ohms at -9.0 volts, to -7.15 ohms at -10 volts, to -10.1 ohms at -11.0 volts.

The diode impedances, Z_B, plotted in Figure 6.2 are the packaged diode impedances. Using the model shown in Figure 6.3 the InP device impedance was further de-embedded from the package parasitics. The chip was modeled using a series resistance and a reactance. The values of R and X calculated from the packaged diode impedance for the case of -11.0 volts bias of Figure 6.2 are plotted in Figure 6.4 against 1/f for frequencies ranging from 30 to 39 GHz. From a least squares fit of X vs 1/f data a series capacitance of 0.17 pF was derived. Thus, this device can be represented by a series resistance of -4.35 ohms and a capacitance of 0.17 pF over the frequency range from 30 to 39 GHz. Using the expression $1/\omega RC$ for the Q of a series R and C

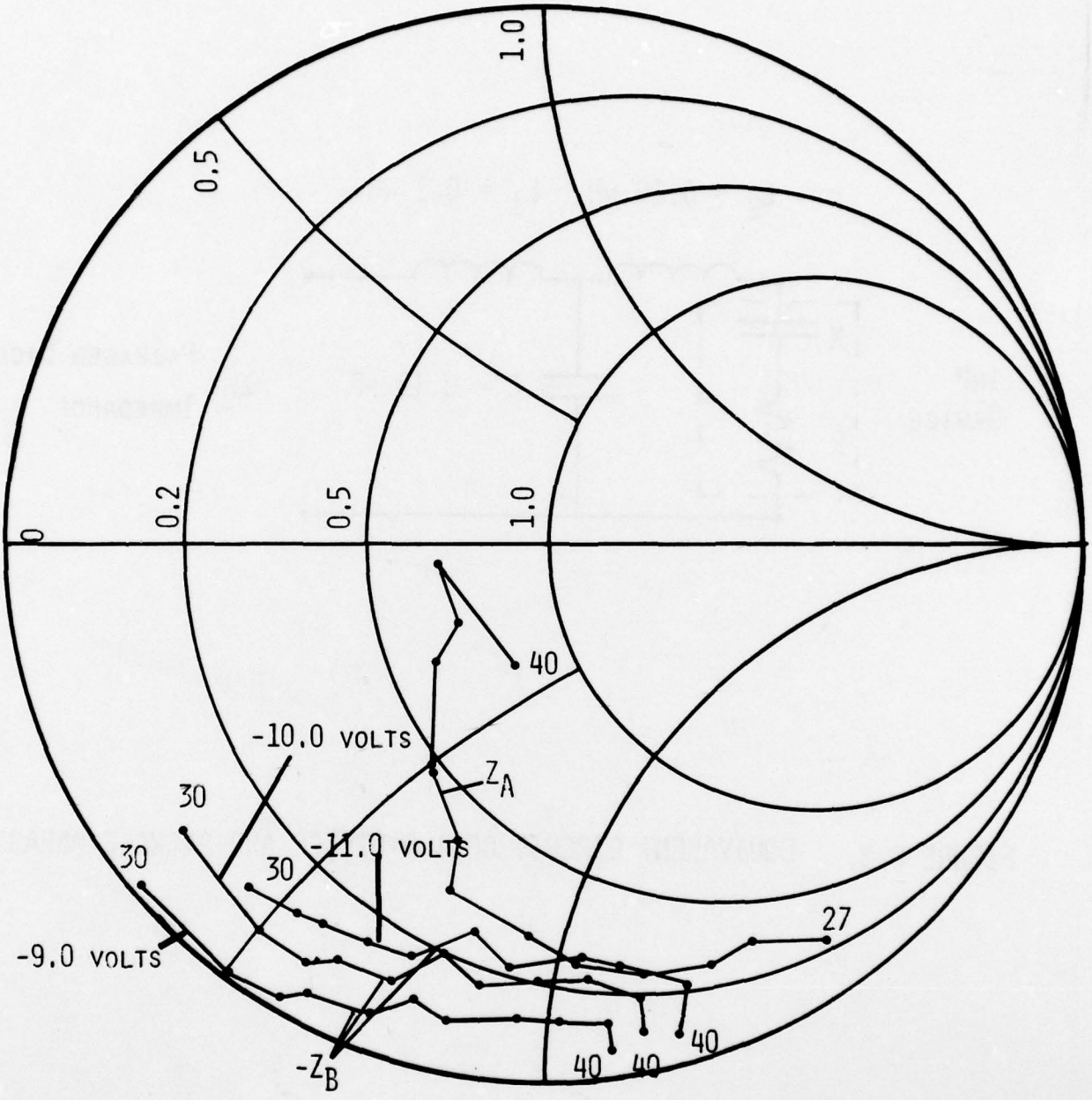


FIGURE 6.2 CIRCUIT IMPEDANCE Z_A AND NEGATIVE OF DIODE IMPEDANCE Z_B AT THREE DIFFERENT BIAS LEVELS AS A FUNCTION OF FREQUENCY

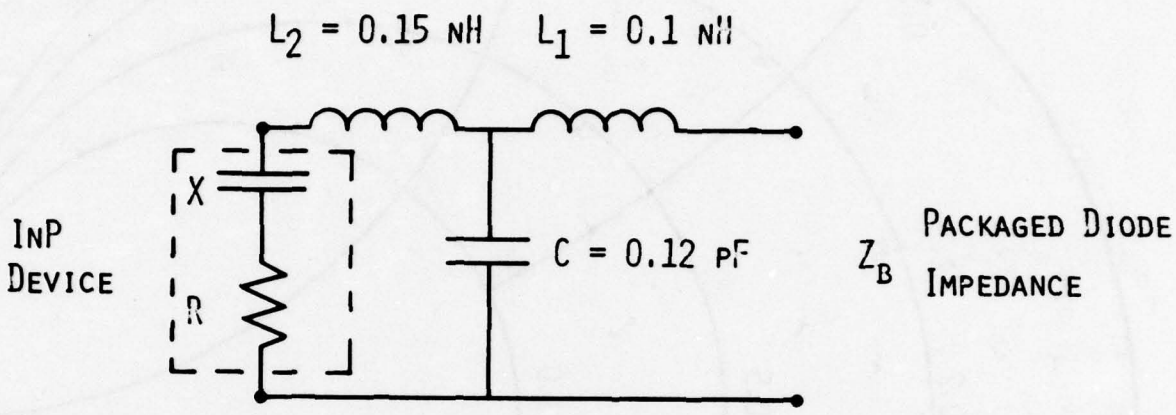


FIGURE 6.3. EQUIVALENT CIRCUIT OF INP DEVICE AND PACKAGE PARASITICS

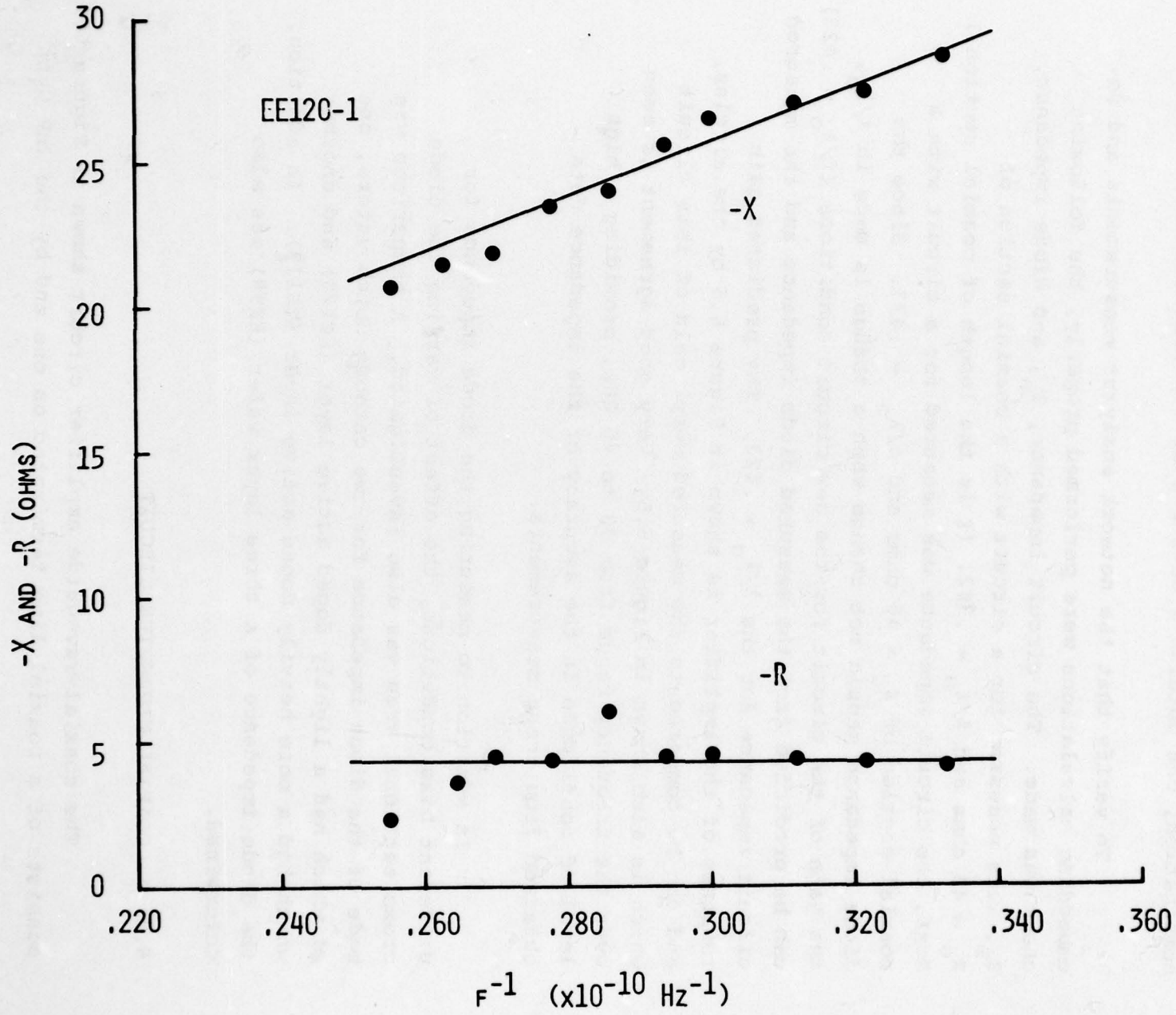


FIGURE 6.4 NEGATIVE RESISTANCE AND REACTANCE OF InP DEVICE VERSUS 1/F

combination, one obtains a device Q of 6.1 evaluated at 35 GHz.

To verify that the network analyzer measurements and de-embedding calculations were performed properly, the following check was made. The circuit impedance, Z_A, and diode impedance, Z_B, were measured for a circuit with a coaxial section of Z_o = 40 ohms and ℓ/λ_o = .392. (ℓ is the length of coaxial section.) Next, the circuit impedance was measured for a circuit with a coaxial section of Z_o = 40 ohms and ℓ/λ_o = .423. Since the diode impedance should not change when a change is made in ℓ/λ_o, the gain of the circuit for the new circuit conditions (ℓ/λ_o = .423) can be predicted from the measured diode impedance and the measured circuit impedance for the ℓ/λ_o = .423. The predicted gain response of the amplifier is shown in Figure 6.5 by the circles, and can be compared to the measured swept gain of this circuit which is also shown in Figure 6.5. Very good agreement is seen over the frequency range from 30 to 40 GHz, providing a high level of confidence in the accuracy of the impedance data obtained from these measurements.

In addition to measuring the diode impedance for different bias conditions, the effect of varying the diode cross sectional area was also investigated. A comparison was made of the diode impedance for two cathode notch wafers, one of which had a lightly doped active layer (EE120) and another which had a more heavily doped active layer (EE119). In addition, the diode impedance of a three layer wafer (EE98) was also determined.

6.2 COAXIAL WAVEGUIDE CIRCUIT

The coaxial waveguide amplifier circuit shown in Figure 6.1 consists of a coaxial line terminated on one end by the InP Gunn

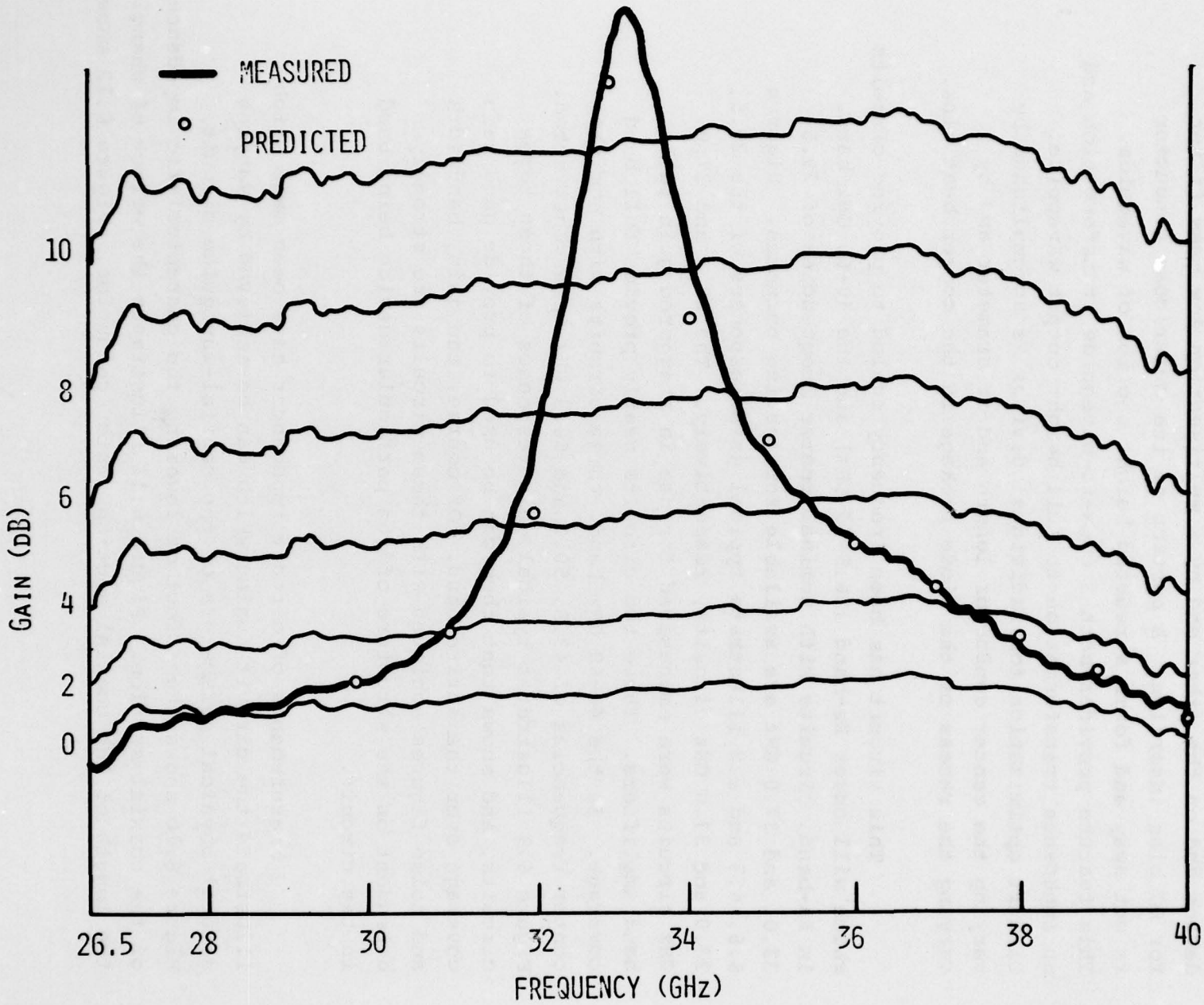


FIGURE 6.5 COMPARISON OF MEASURED GAIN RESPONSE AND THAT PREDICTED FROM IMPEDANCE MEASUREMENTS

device and on the other end by a multisection low pass filter for DC bias insertion. A portion of the outer coax conductor is cut away and forms a reduced height section of waveguide. This feature provides both a coax-to-waveguide transformation and an impedance transformation to full height output waveguide. Circuit optimization for individual devices is accomplished by varying the center conductor length and/or diameter and by varying the recess of the diode package in the copper heat sink.

This circuit has been frequency scaled to provide circuits which will cover Ka-band (26.5-40 GHz) and the 40-60 GHz band. In Ka-band, circuits with nominal center frequencies of 29.5, 33.0, and 37.0 GHz are available for testing purposes. Figures 6.6, 6.7 and 6.8 illustrate typical gain responses of the 29.5, 33.0 and 37.0 GHz circuits, respectively. The 29.5 and 37.0 GHz circuits were emphasized for use in staggered gain full band amplifiers. These two circuits nearly provide full band coverage. In the 40-60 GHz band, three circuits with nominal center frequencies of 43.5, 50.0 and 56.5 GHz were constructed. Figure 6.9 illustrates typical gain responses of these three circuits, and shows that they can be used to provide good gain coverage over the entire band. Of course, the gain, bandwidth and noise figures achieved with these circuits are strongly dependent on the structure of the particular device being used in the circuit.

Measurements of circuit impedances have been made which illustrate the circuit tuning which can be achieved by varying several physical parameters of the coaxial-waveguide circuit. Figure 6.10 shows the effect of lowering the characteristic impedance of the coaxial section. Figure 6.11 illustrates the effect of changing the length of the coaxial section center conductor. Figure 6.12 shows

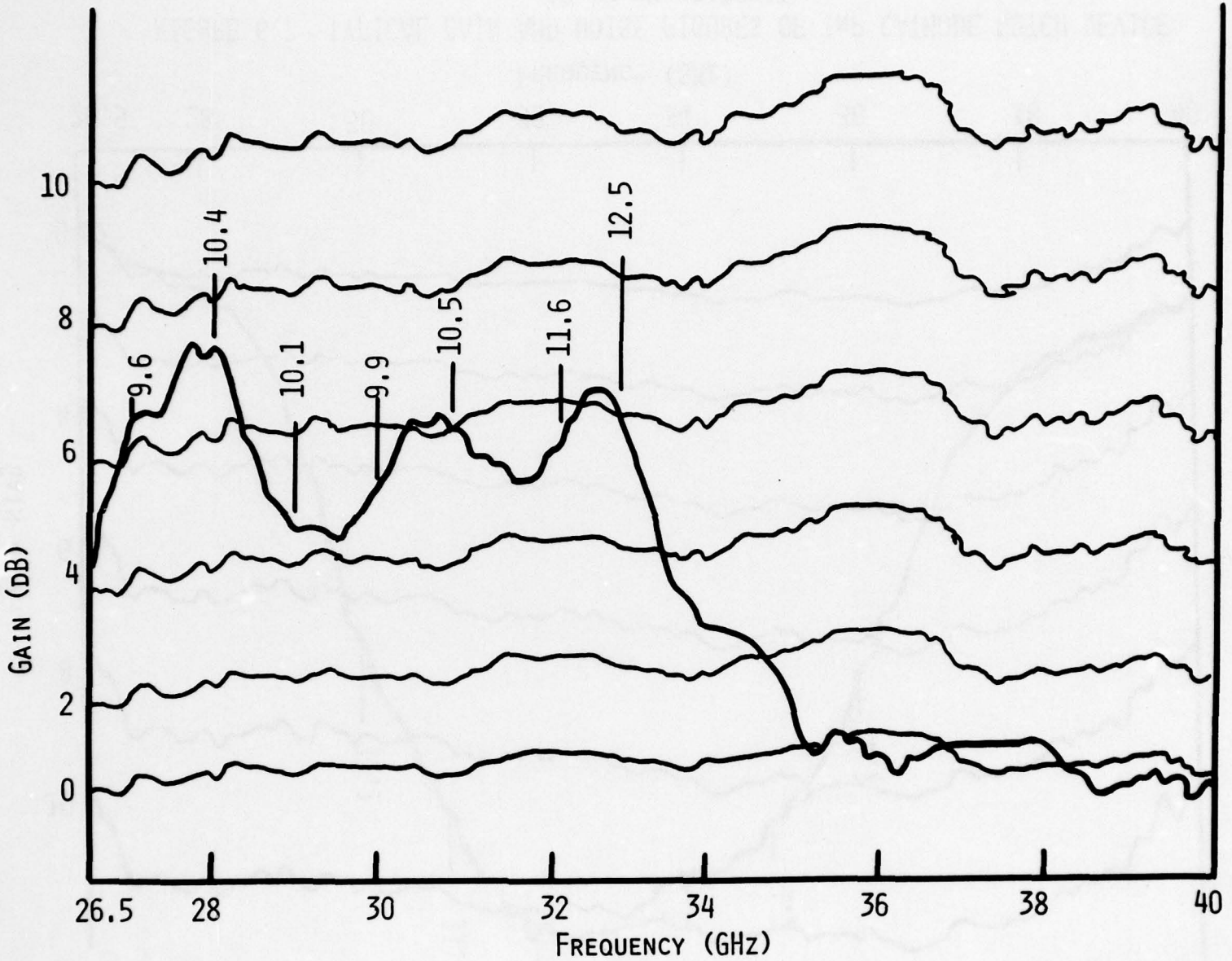


FIGURE 6.6 TYPICAL GAIN RESPONSE OF InP CATHODE NOTCH DEVICE IN 29.5 GHz CIRCUIT

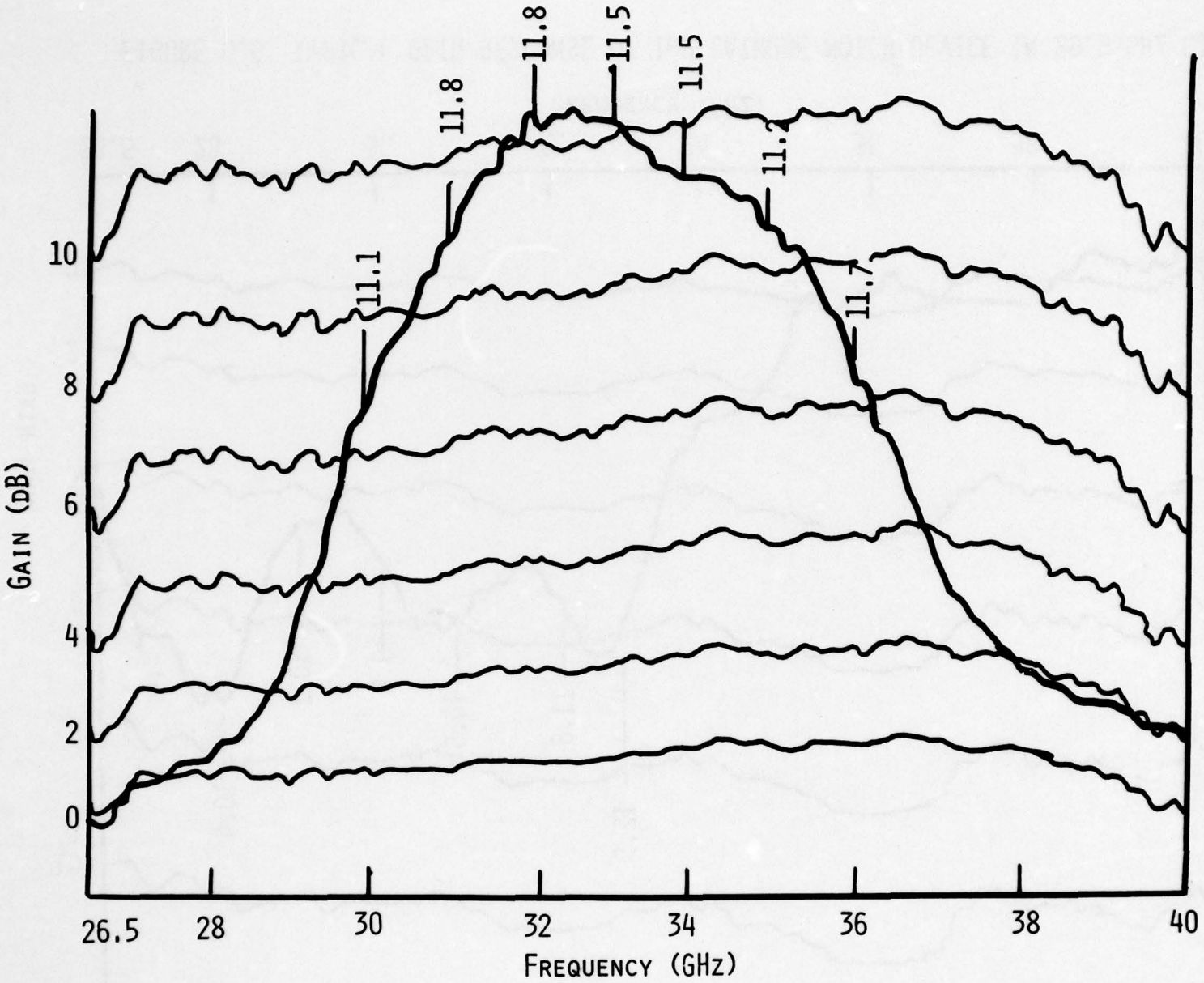


FIGURE 6.7 TYPICAL GAIN AND NOISE FIGURES OF InP CATHODE NOTCH DEVICE IN 33 GHz CIRCUIT

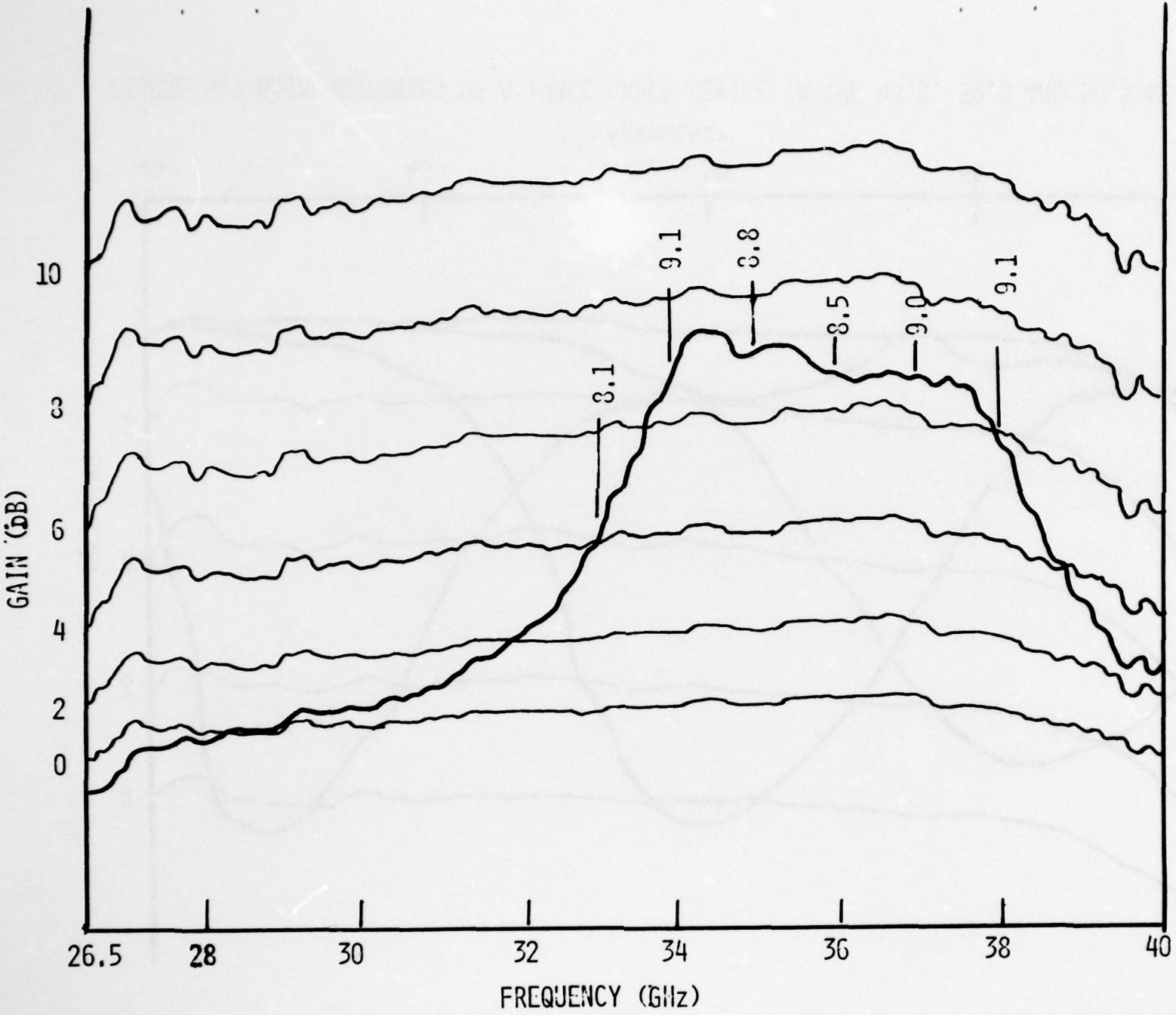


FIGURE 6.8 TYPICAL GAIN AND NOISE FIGURES OF InP CATHODE NOTCH DEVICE IN 37 GHz CIRCUIT

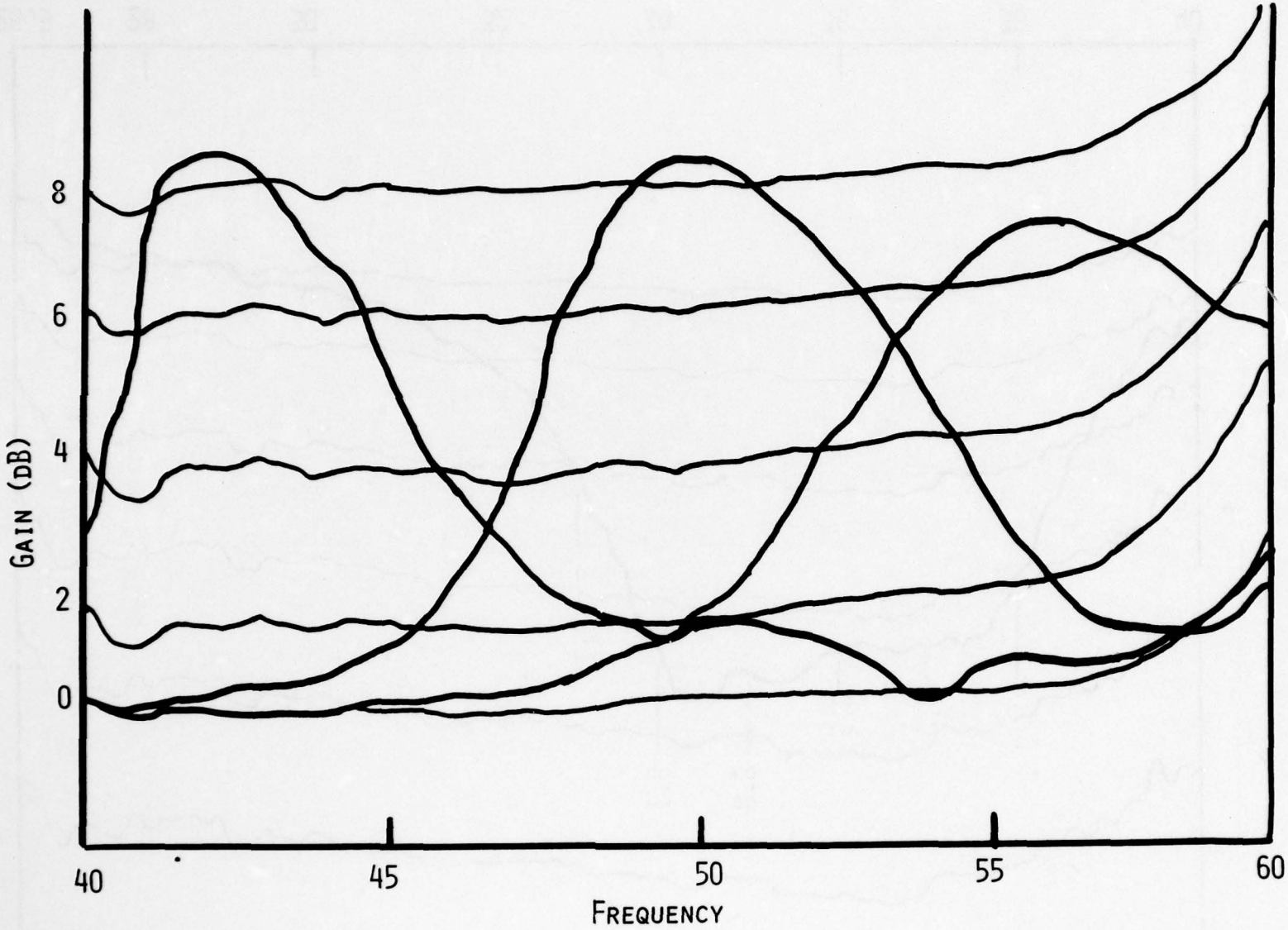


FIGURE 6.9 GAIN RESPONSES OF A THREE LAYER DEVICE IN THE 43.5, 50.0 AND 56.5 GHz CIRCUIT

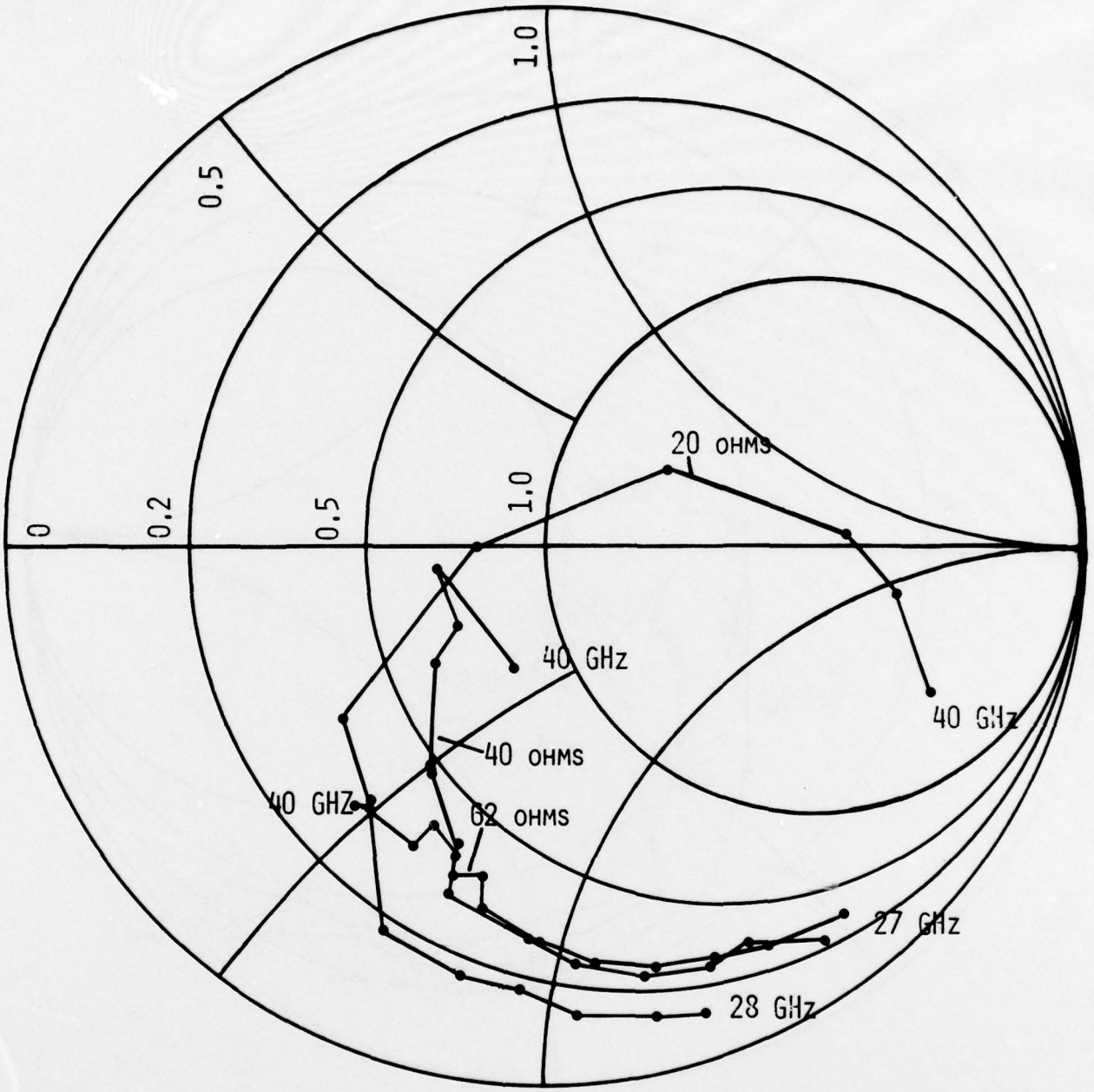


FIGURE 6.10. CIRCUIT IMPEDANCES VS FREQUENCY FOR THREE DIFFERENT COAXIAL SECTION CHARACTERISTIC IMPEDANCES

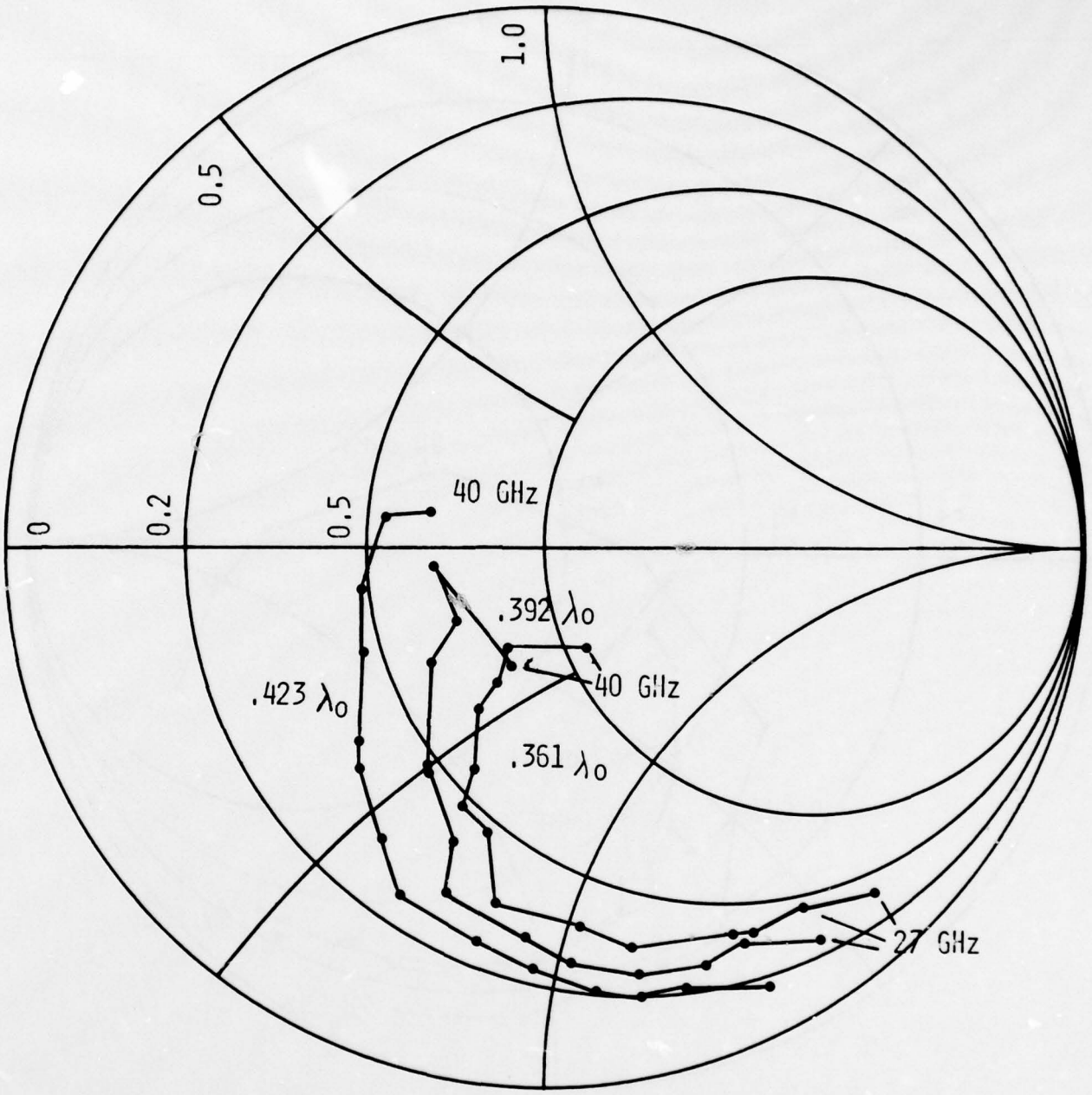
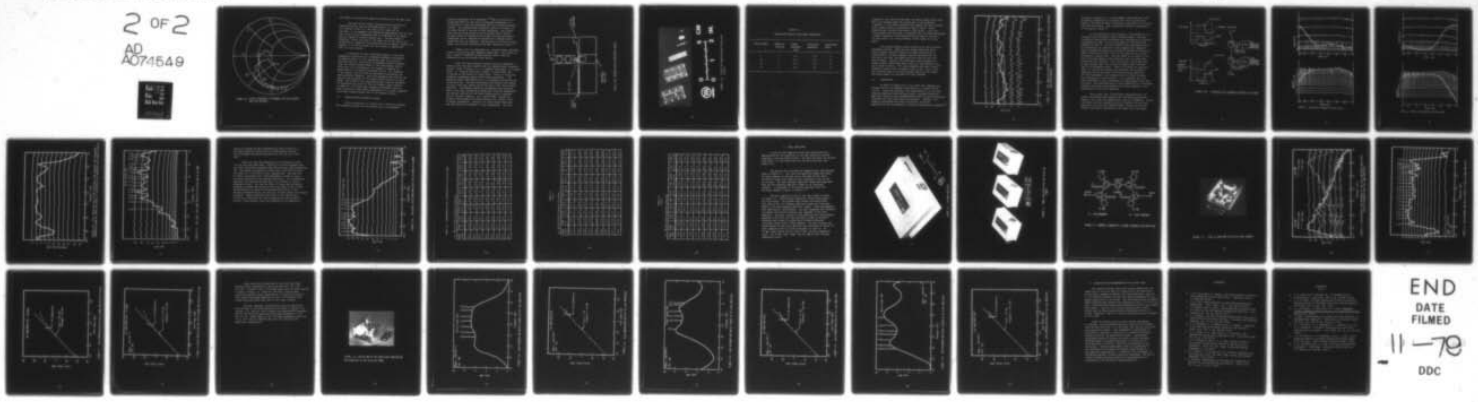


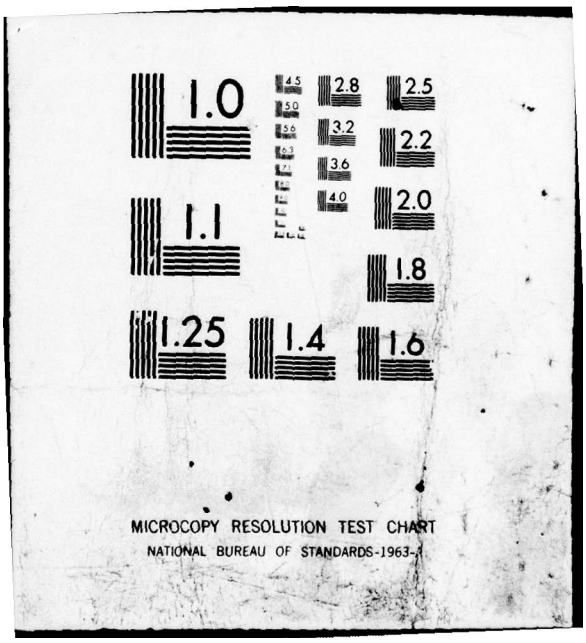
FIGURE 6.11. CIRCUIT IMPEDANCES VS FREQUENCY FOR THREE DIFFERENT LENGTHS OF COAXIAL SECTION

AD-A074 549 VARIAN ASSOCIATES PALO ALTO CA CENTRAL RESEARCH LAB F/G 9/5
INDIUM PHOSPHIDE GUNN DEVICES (26-60GHZ).(U)
AUG 79 J D CROWLEY, S B HYDER, B R CAIRNS N00123-77-0459
UNCLASSIFIED NOSC-TD-275 NL

2 OF 2
AD A074549



END
DATE FILMED
11-79
DDC


1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
4.5
5.0
5.6
6.3
7.1
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

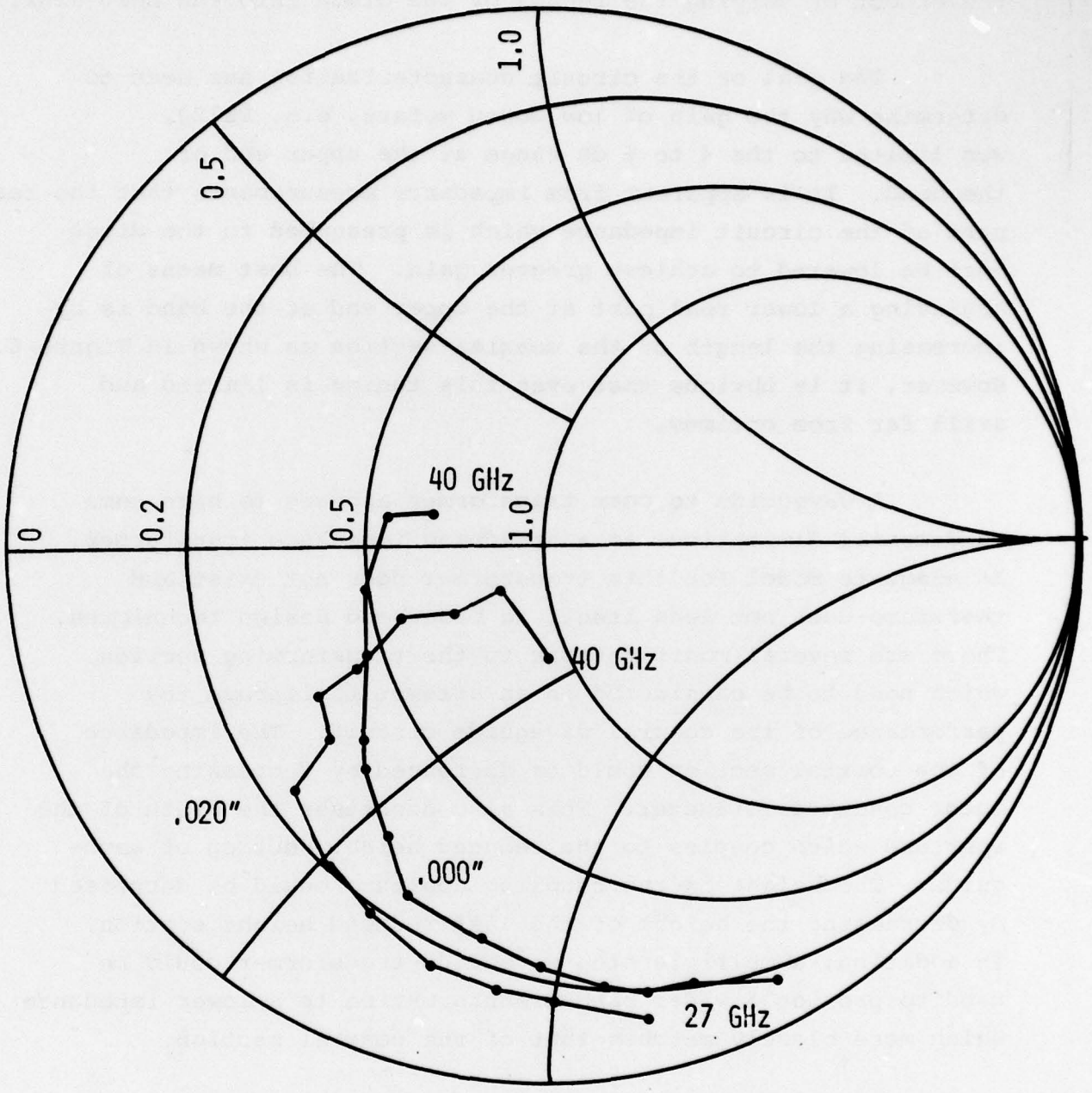


FIGURE 6.12. CIRCUIT IMPEDANCES VS FREQUENCY FOR TWO DIFFERENT HEAT SINK RECESSES

the effect of varying the recess of the diode into the heat sink.

The goal of the circuit characterization has been to determine why the gain of low doped wafers, e.g. EE120, was limited to the 4 to 6 dB range at the upper end of the band. It is apparent from impedance measurements that the real part of the circuit impedance which is presented to the diode must be lowered to achieve greater gain. The best means of achieving a lower real part at the upper end of the band is by increasing the length of the coaxial section as shown in Figure 6.11. However, it is obvious that even this tuning is limited and still far from optimum.

A waveguide to coax transformer appears to have some fundamental limitations as a broadband impedance transformer. An adequate model for this transformer does not exist and therefore does not lend itself to broadband design techniques. There are several modifications to the transforming section which need to be considered in an attempt to improve the performance of the coaxial waveguide circuit. The impedance of the coaxial section could be decreased by decreasing the outer conductor diameter. This also decreases the width of the aperture which couples to the reduced height section of waveguide. The height of the coupling aperture could be decreased by decreasing the height of the last reduced height section. In addition, a multiple step waveguide transformer could be used to provide a wider band transformation to a lower impedance which more closely matches that of the coaxial section.

6.3 REDUCED HEIGHT WAVEGUIDE CIRCUIT

The full potential of a given T.E.A. device for maximum gain bandwidth product can be realized only if broad-band

matching techniques can be employed.[11,12] Due to the lack of a broad band model for the coax to waveguide transformer, it is difficult to use such techniques with the coaxial-waveguide circuit. The reduced height waveguide circuit of Figure 6.13 is better suited to the use of such techniques. The sliding short and the diode recess into the reduced height section provide a means of resonating the diode, and the multisection transformer can be designed to provide the broadband filter properties that are required. Optimization of a similar circuit using a two section transformer has been reported by Rubin.[13]

Figure 6.14 is a photograph of a reduced height waveguide circuit with a three step impedance transformer. Using this circuit, a gain$^{1/2}$ bandwidth product greater than 27 GHz was obtained with an InP cathode notch device.

There are five principal factors which are important in obtaining the wide band results from the reduced height waveguide circuit shown in Figure 6.13: a) stepped transformer; b) sliding short; c) vertical position of diode; d) bias choke; and e) joining of two halves of circuit body. Table 6.1 lists four different transformer designs which were constructed . The design of these transformers did not incorporate corrections for discontinuities. The best performance was achieved with design II, and it was this version which was used in the final Ka-band amplifier. Considerable empirical adjustments were required until a low loss, contacting sliding short could be implemented. The vertical position of the diode flange plays an important role in the gain response. For a given diode, raising the flange in the waveguide increases the gain and causes a shift to higher frequencies. Lowering the diode flange lowers the gain and shifts the response to lower frequencies. For gain

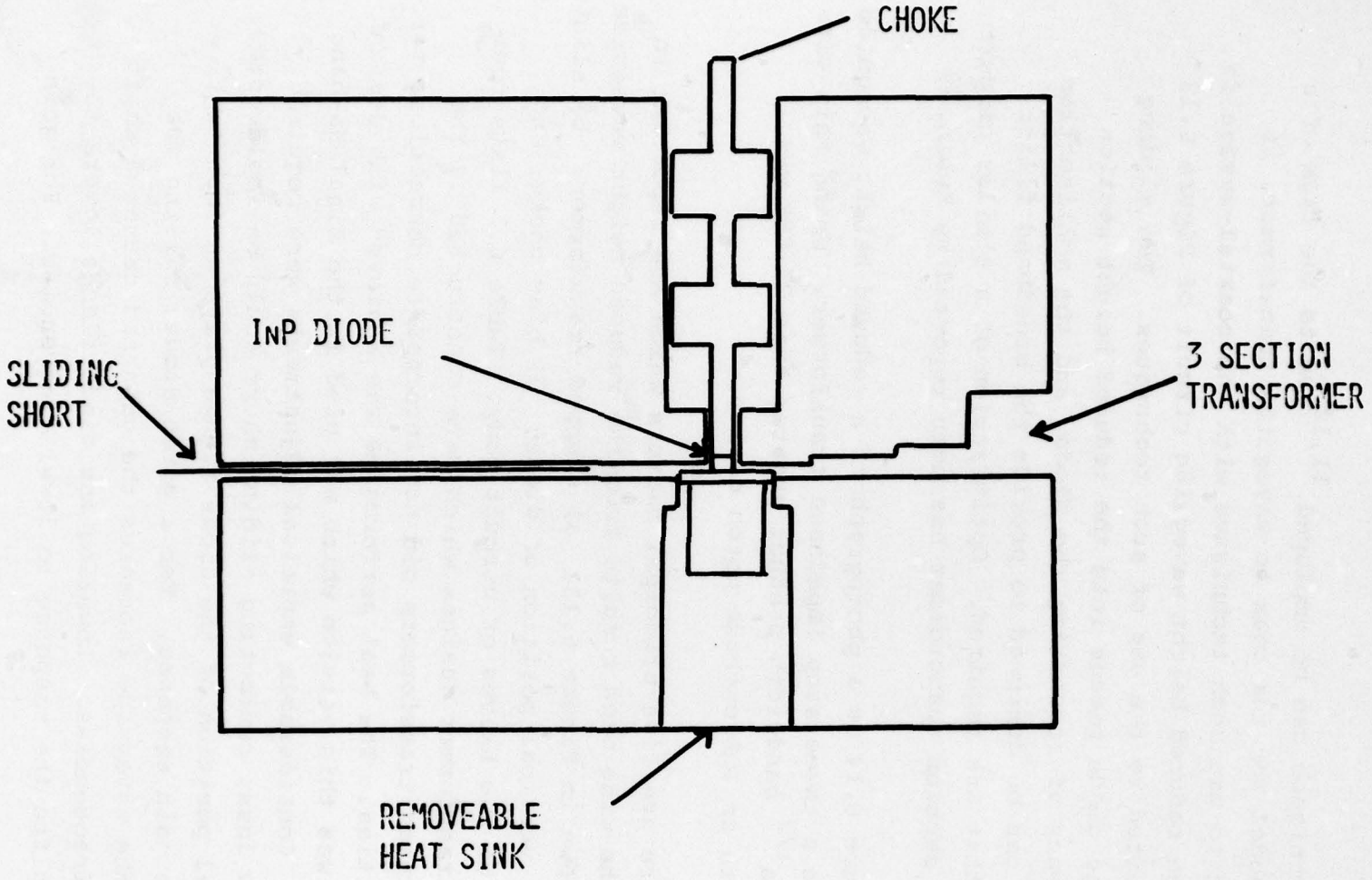
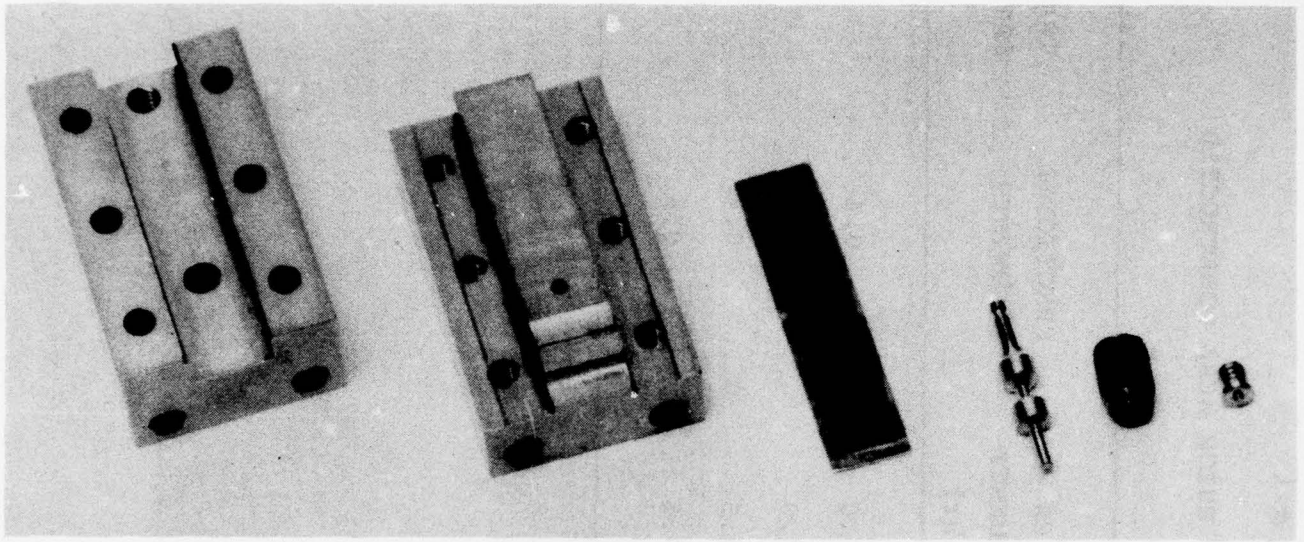


FIGURE 6.13 REDUCED HEIGHT WAVEGUIDE CIRCUIT



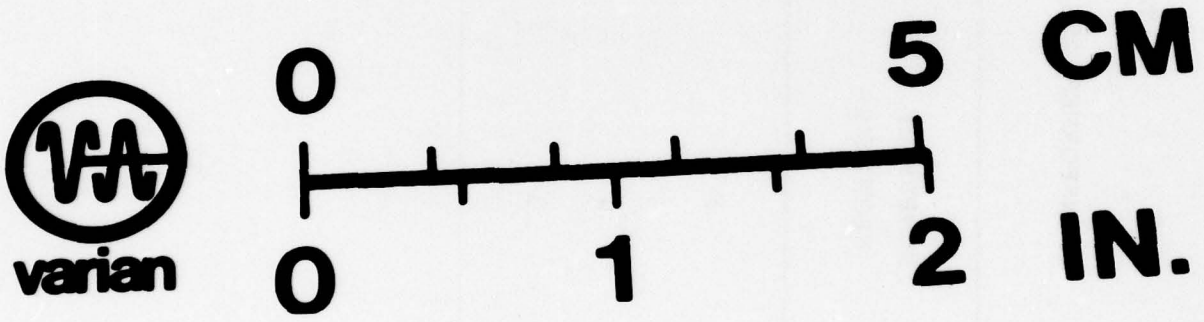


FIGURE 6.14 35 GHz InP Reduced Height Oscillator Circuit

TABLE 6.1

TRANSFORMER DESIGNS WHICH WERE CONSTRUCTED

DESIGN NUMBER	NUMBER OF SECTIONS	CENTER FREQUENCY (GHz)	FRACTIONAL BANDWIDTH	TRANSFORMER RATIO
I	3	37.0	0.4	15
II	3	37.0	0.4	14
III	3	29.5	0.4	14
IV	3	29.5	0.8	10

response at the low end of Ka-band, the diode flange often times had to be recessed below the bottom wall of the waveguide. A dumbbell rf bias choke provided less leakage than that achieved with a tight fitting, insulated pin type of choke. These reduced height circuits were made in two halves. A low loss joint between the two halves is important for wide band performance. A highly conductive filler material must be used to achieve a low loss joint, e.g. silver brazing, silver epoxy, or silver paint.

This reduced height circuit proved to be very versatile throughout Ka-band. Using the two tuning mechanisms which were available (vertical position of diode and position of sliding short) the gain response could be optimized for the low end of the band, the upper end of the band or even full band coverage. Figure 6.15 illustrates a gain response of a single cathode notch diode which gives full band coverage in one of these circuits. This gain response represents a gain$^{1/2}$ bandwidth product which is greater than 27 GHz. Each of the four circuits used in the final Ka-band amplifier was tested and shown capable of providing this same coverage.

6.4 CIRCULATORS

As shown in Figure 6.15, a full band gain response was achieved with an InP cathode notch device in a reduced height circuit. Using this amplifier, the construction of a full band, high gain amplifier using multiple stage, cascaded reflection amplifiers would be very straightforward with full band circulators. Currently only half band units are available. However, with properly constructed half band circulators, full band amplification can be achieved by using the staggered gain approach [14]

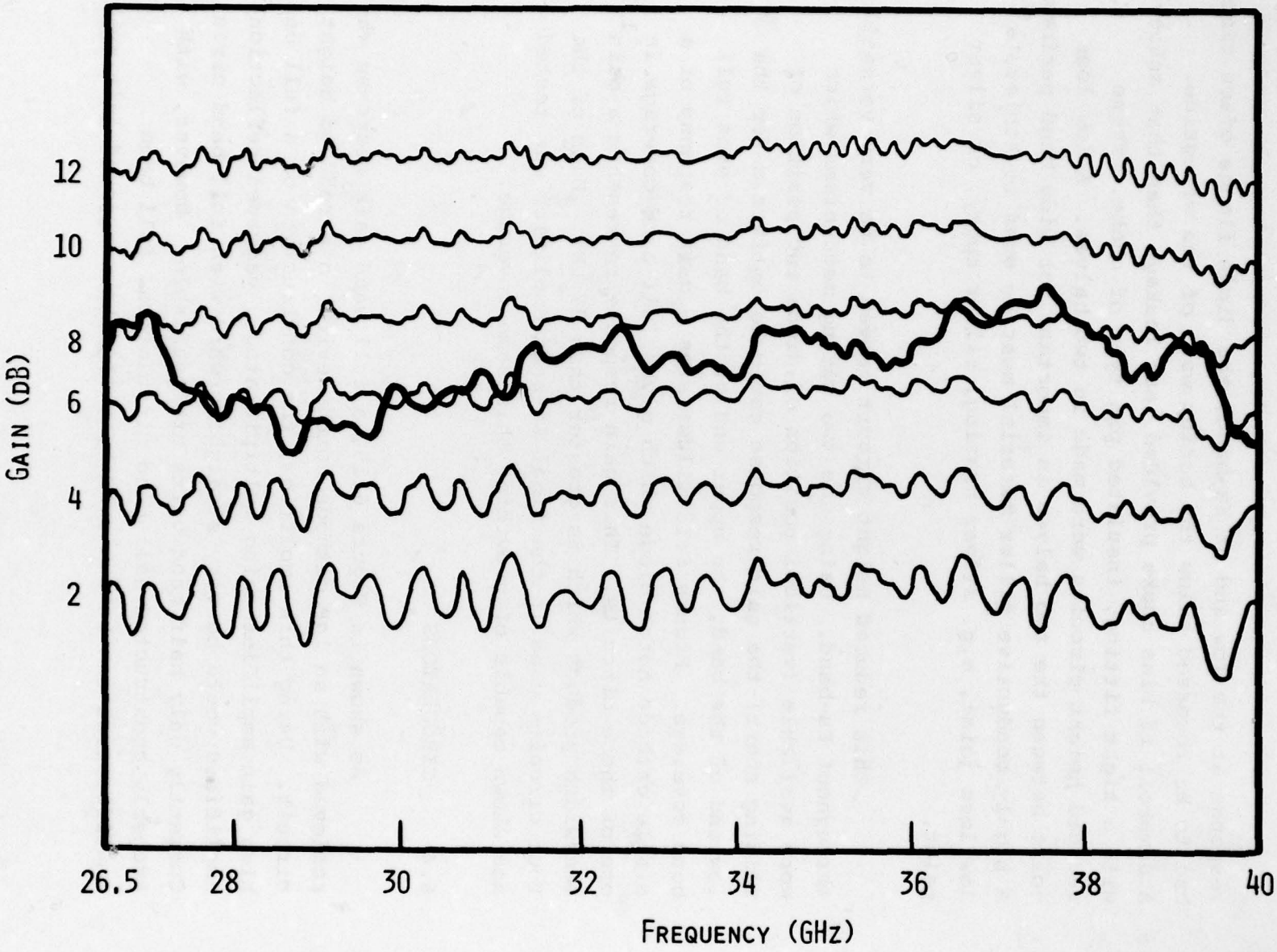


FIGURE 6.15. FULL BAND GAIN RESPONSE OF SINGLE InP CATHODE NOTCH DEVICE MEASURED WITH REFLECTOMETER

as shown in Figure 6.16. In the staggered gain approach, good circulation properties are required only over half the band. However, care must be taken to maintain a good match at all ports over the entire band. Such circulators have been constructed in the past at Varian.[15]

At the beginning of this program, it was decided to try to obtain such circulators from an outside vendor. The best circulators which could be obtained were manufactured by Aertech, a subsidiary of TRW. Initial development of circulators was conducted at TRW. [16] For each stage of full band amplification two circulators are required in the staggered gain approach. Typical performance which was achieved by Aertech circulators is shown in Figures 6.17 and 6.18, for the high end and low end circulators, respectively. The poor match at all ports at one end of the band leads to high insertion loss and ripple when circulators are cascaded. The "out-of-band" return loss must be kept greater than 8 dB to keep the double pass insertion loss at an acceptable level. Figure 6.19 shows the insertion loss of the two circulators, one isolator, two circulator combination which was used in the final Ka-band amplifier. For this measurement, each amplifier port of each circulator was terminated in a short circuit. It is apparent that the useful bandwidth of this combination is significantly less than full band. The characteristics of this combination of circulators severely restricted the bandwidth of the gain response in the construction of the final amplifier.

Due to their poor "out-of-band" characteristics, the Aertech circulators were marginal for full band applications. However, for a half band application, they are acceptable. Figure 6.20 shows the gain response and noise figures of a two stage amplifier which uses two reduced height circuits and the two Aertech circulators optimized for the upper end of the band.

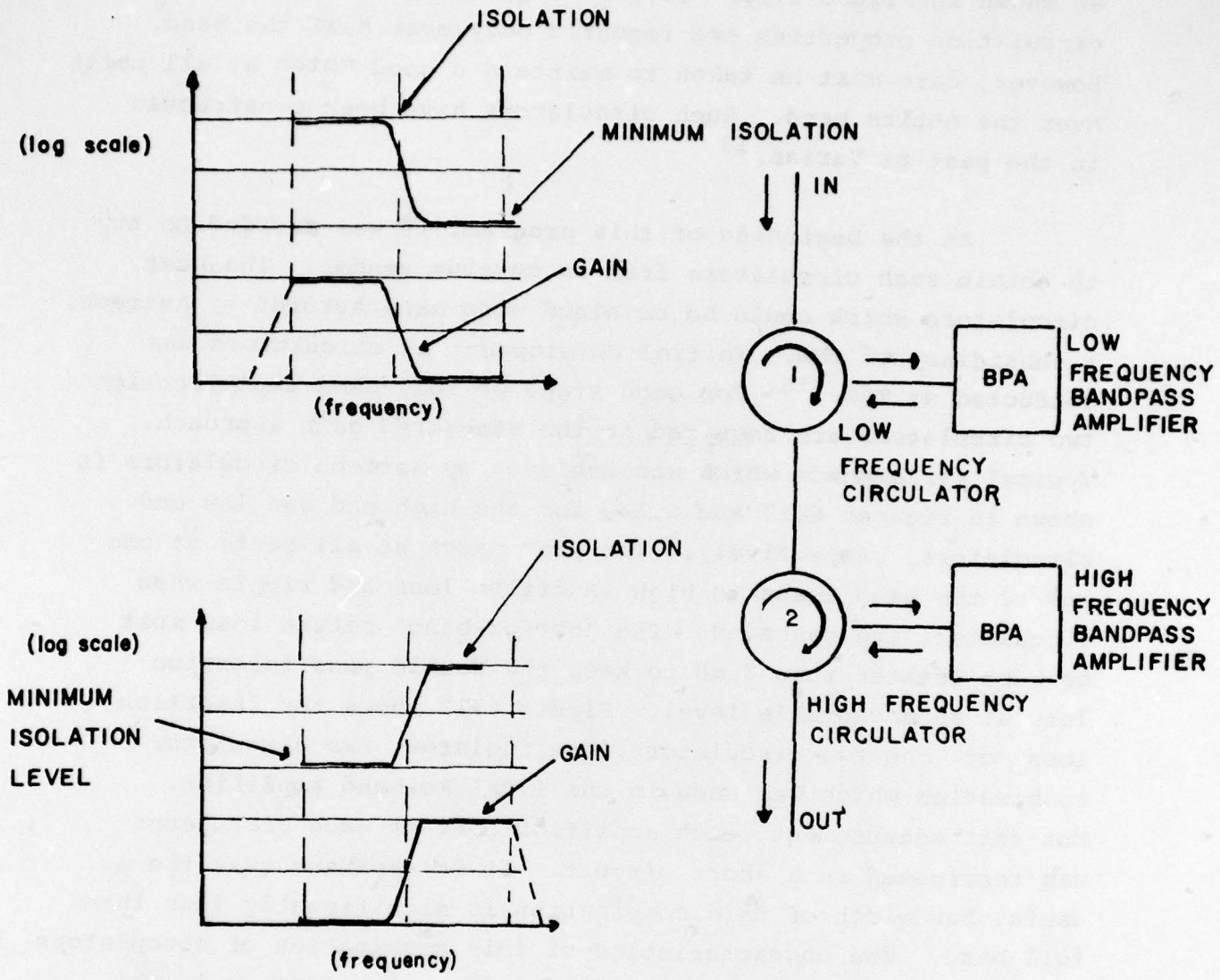


FIGURE 6.16. STAGGERED GAIN TECHNIQUE EMPLOYED IN KA-BAND

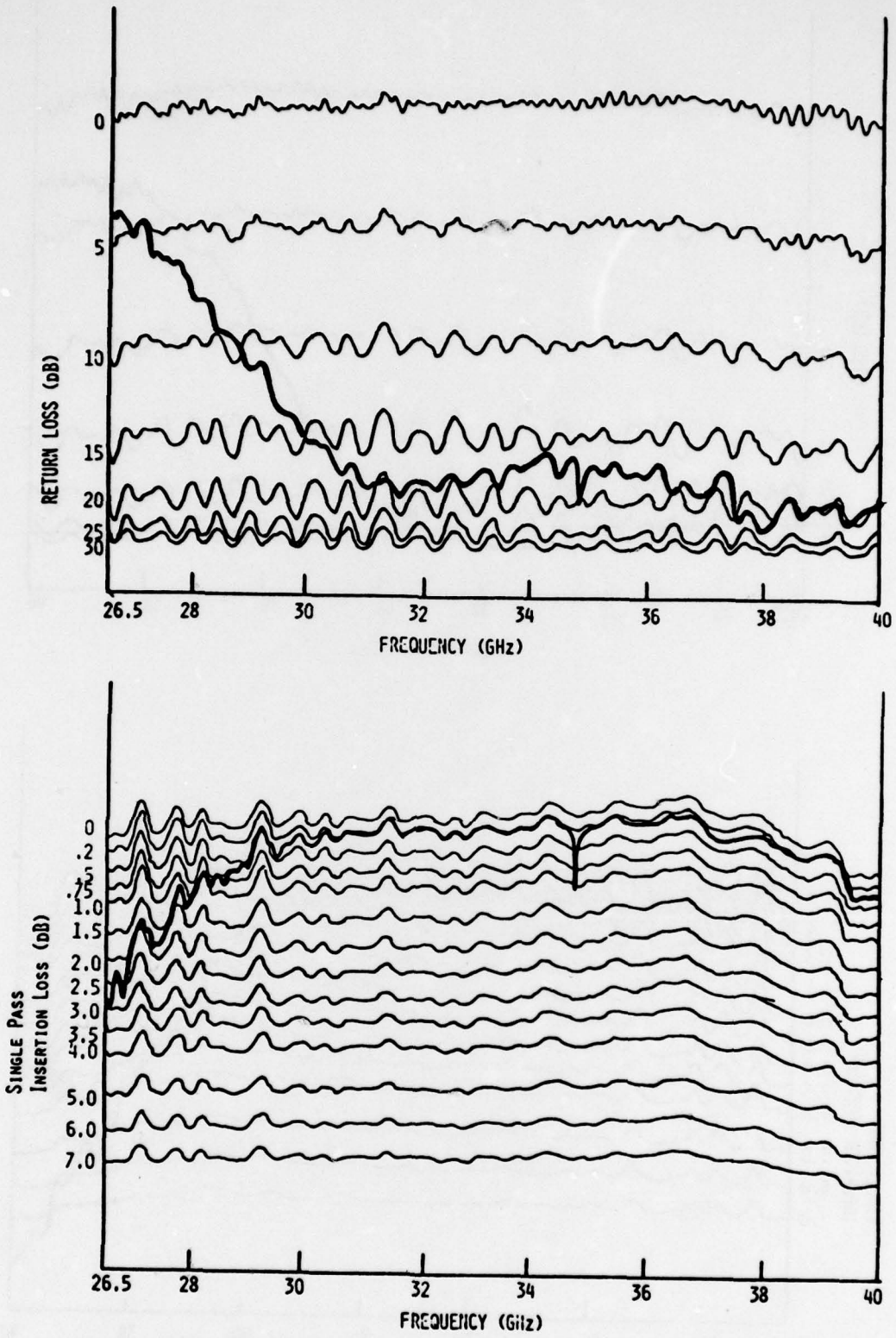
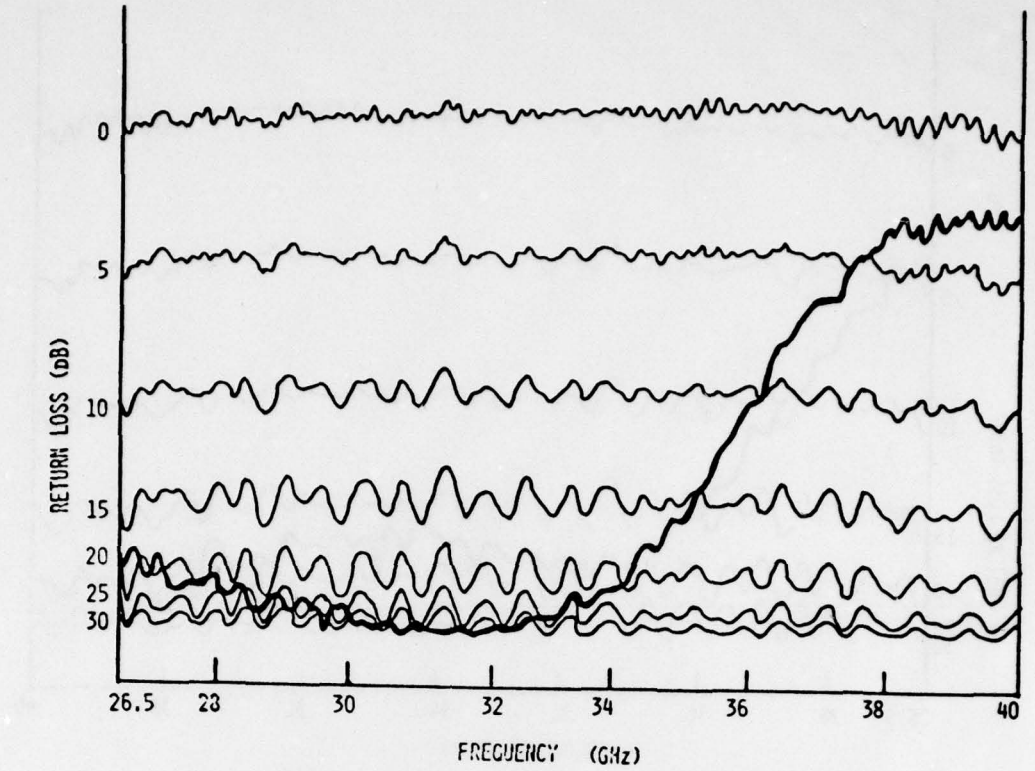


FIGURE 6.17 INSERTION LOSS OF CIRCULATOR FOR HIGH END OF KA-BAND



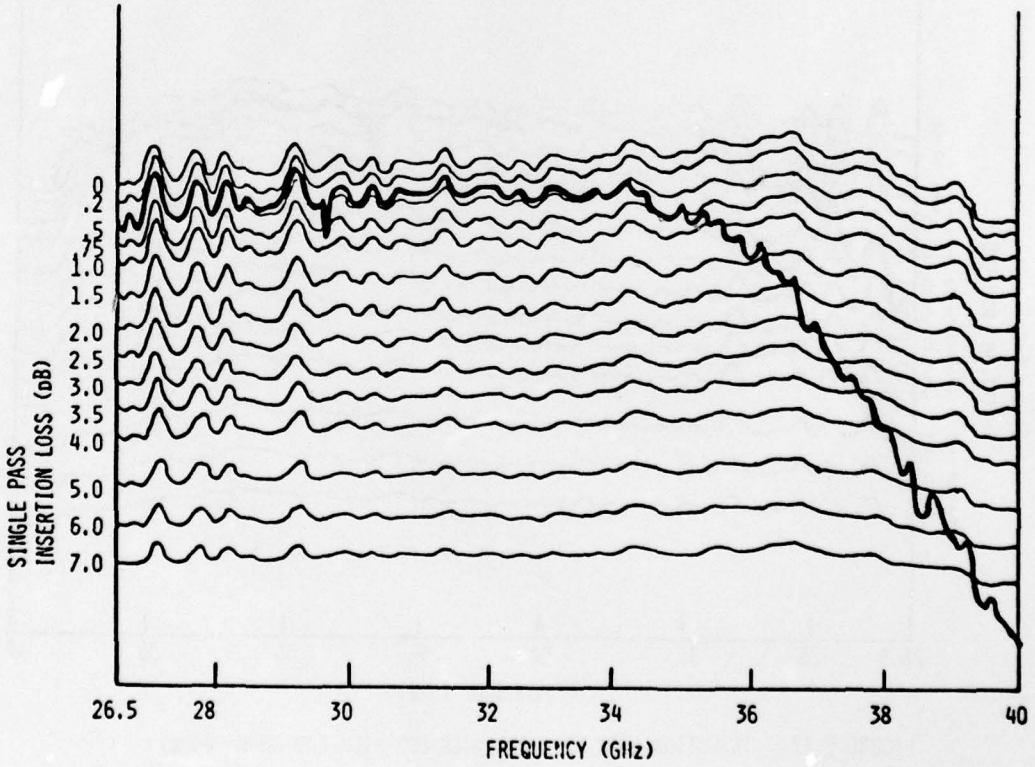


FIGURE 6.18 INSERTION LOSS OF CIRCULATOR FOR LOW END OF KA-BAND

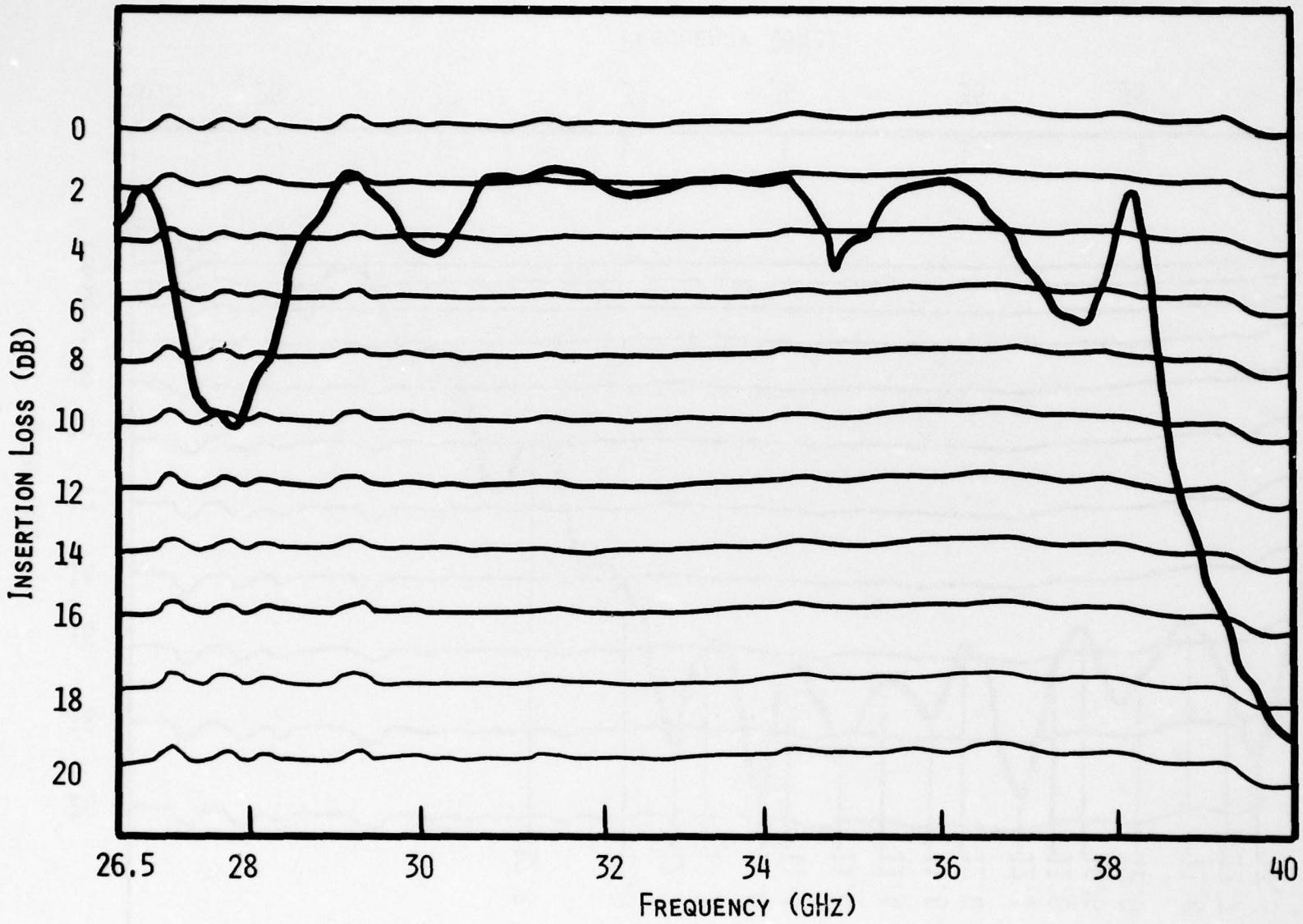


FIGURE 6.19. TOTAL INSERTION LOSS OF TWO CIRCULATOR, ONE ISOLATOR, TWO CIRCULATOR COMBINATION WHEN ALL AMPLIFIER PORTS OF CIRCULATORS ARE TERMINATED WITH SHORT CIRCUITS

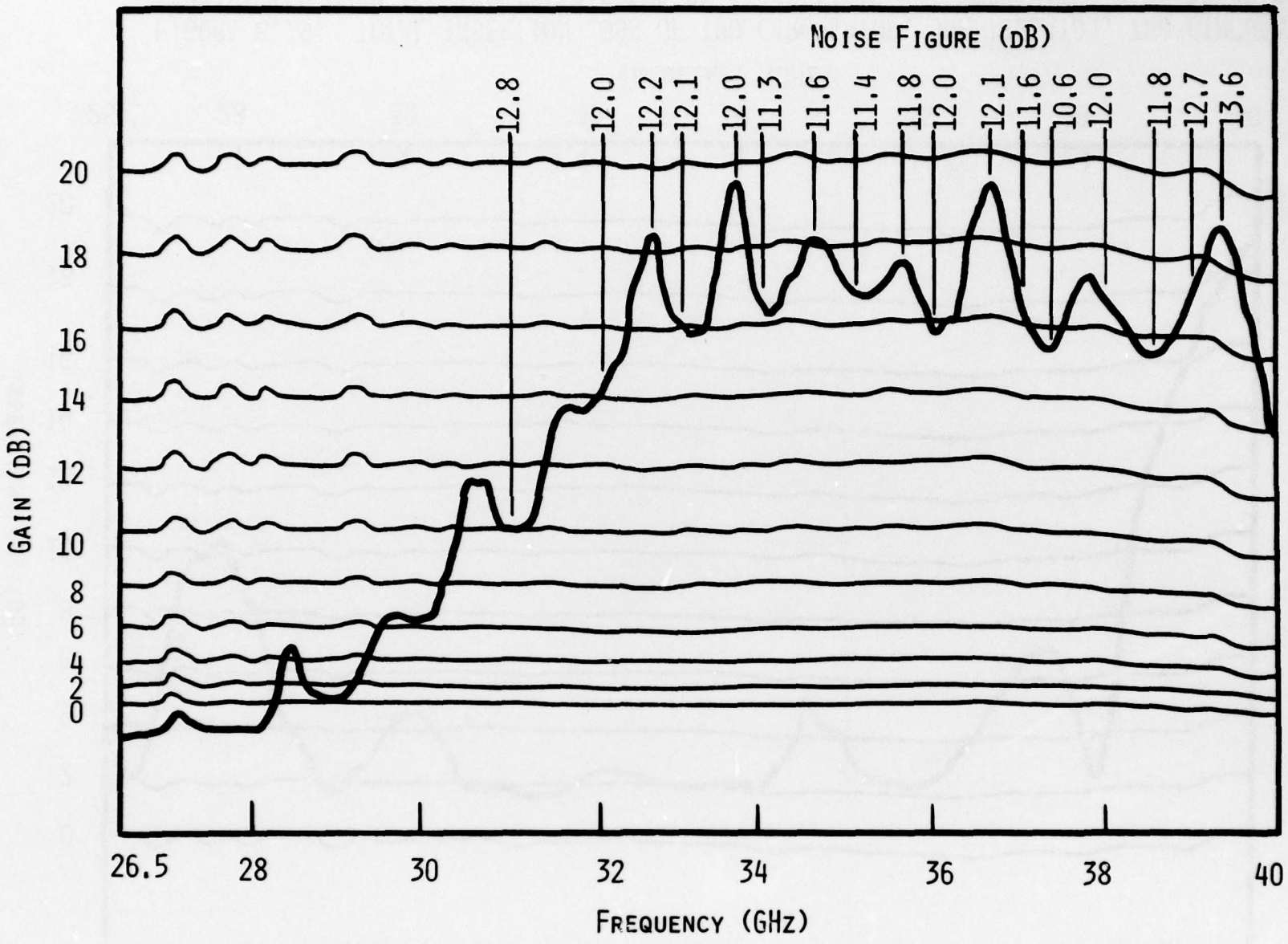


FIGURE 6.20. TWO STAGE, HALF BAND AMPLIFIER FOR HIGH END OF KA-BAND

Figure 6.21 shows the gain responses and noise figures of a two stage amplifier which uses two reduced height circuits and two Aertech circulators optimized for the low end of the band.

There are very few manufacturers of wide-band circulators for the 40-60 GHz range. Table 6.2 lists the measured data for three circulators purchased from TRG Division, Alpha Industries, Inc. The center frequencies of these three Y-junction circulators were 43.5, 50.0 and 56.5 GHz, respectively. The goal was to obtain circulators with 7 GHz bandwidths in order to cover the entire band with three separate amplifiers. For a reflection amplifier the VSWR must be less than 1.22 in order to obtain acceptable ripple. The data of Table 6.2 shows that the useful bandwidth of these TRG circulators was only about 4 GHz at best. The performance of these TRG circulators falls short of the desired performance goals, but they are the best which are currently available. These circulators were used in the construction of the final amplifiers for this program and as can be seen in Section 7 they severely limit the bandwidth of the amplifiers.

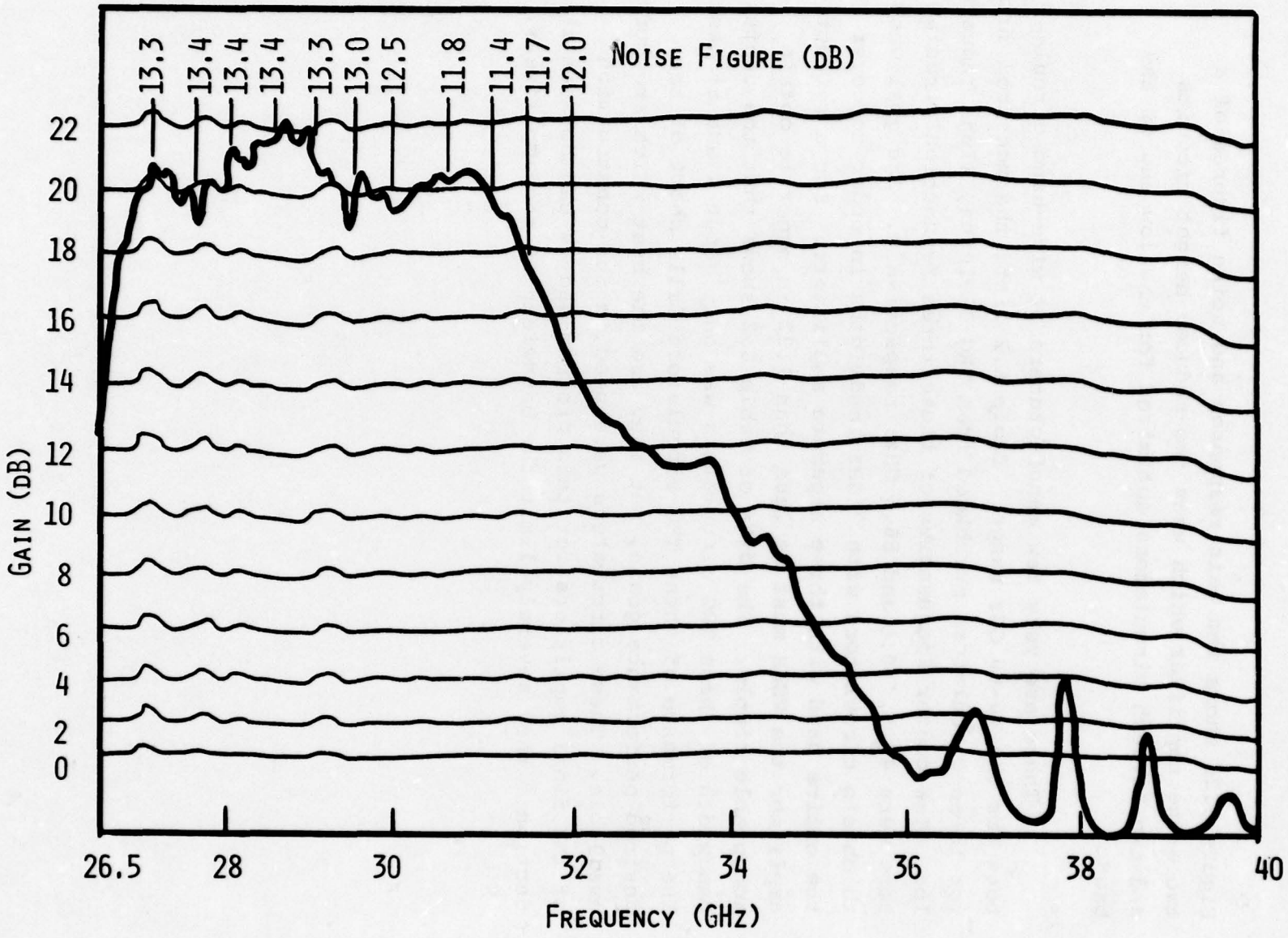


FIGURE 6.21. TWO-STAGE, HALF BAND AMPLIFIER FOR LOW END OF KA-BAND

TABLE 6.2. PERFORMANCE OF TRG CIRCULATORS FOR 40-60 GHz RANGE

A. TRG 43.5 GHz Y-Junction Circulator

FREQ. (GHz)	VSWR (1)	LOSS (1-2)	ISOL. (1-3)	VSWR (2)	LOSS (2-3)	ISOL (2-1)	VSWR (3)	LOSS (3-1)	ISOL (3-2)
47.0	1.50	0.5	14.0	1.50	0.4	15.0	1.5	0.5	14.5
46.0	13.8	0.4	17.0	1.38	0.4	17.0	1.35	0.4	16.5
45.0	12.0	0.4	20.0	1.22	0.4	21.0	1.20	0.4	20.0
44.0	1.10	0.4	24.0	1.10	0.4	>25	1.10	0.4	> 25
43.0	1.10	0.4	25.0	1.10	0.4	>25	1.10	0.4	> 25
42.0	1.15	0.4	20.0	1.20	0.4	22.5	1.12	0.4	22.0
41.0	1.47	0.6	14.0	1.50	0.8	15.0	1.50	0.8	14.5
40.0	1.95	0.9	12.0	1.95	1.0	12.5	1.97	1.0	12.0

TABLE 6.2
(Cont.)

B. TRG 50.0 GHz Y-Junction Circulator

FREQ. (GHz)	VSWR (1)	LOSS (1-2)	ISOL (1-3)	VSWR (2)	LOSS (2-3)	ISOL (2-1)	VSWR (3)	LOSS (3-1)	ISOL (3-2)
53.5	1.55	0.5	18.0	1.38	0.5	17.0	1.44	0.5	16.5
53.0	1.38	0.4	18.0	1.30	0.4	17.5	1.35	0.4	17.0
52.0	1.25	0.4	23.0	1.15	0.4	21.0	1.25	0.4	21.0
51.0	1.15	0.4	25	1.10	0.4	> 25	1.10	0.4	23.5
50.0	1.15	0.4	25	1.10	0.4	> 25	1.10	0.4	23.0
49.0	1.30	0.4	22.0	1.30	0.4	23.0	1.25	0.4	20.0
48.0	1.57	0.5	16.0	1.58	0.5	16.0	1.38	0.5	15.0
47.0	1.70	0.7	14.0	1.67	0.6	14.5	1.62	0.8	13.0
46.5	1.95	0.9	13.4	1.80	0.8	13.5	1.80	1.0	12.5

TABLE 6.2
(Cont.)

C. TRG 56.5 GHz Y-Junction Circulator

FREQ (GHz)	VSWR (1)	LOSS (1-2)	ISOL (1-3)	VSWR (2)	LOSS (2-3)	ISOL (2-1)	VSWR (3)	LOSS (3-1)	ISOL (3-2)
60.0	1.58	1.0	14.0	1.65	0.9	13.5	1.62	0.8	13.5
59.0	1.33	0.7	14.5	1.50	0.7	14.3	1.50	0.7	16.0
58.0	1.20	0.5	17.0	1.30	0.5	17.0	1.30	0.5	19.0
57.0	1.10	0.5	19.0	1.20	0.5	21.0	1.18	0.5	24.0
56.5	1.10	0.5	20.0	1.23	0.5	24.0	1.20	0.5	>25
56.0	1.10	0.5	20.0	1.20	0.5	25.0	1.15	0.5	>25
55.0	1.22	0.5	19.0	1.35	0.5	20.0	1.20	0.5	24.0
54.0	1.38	0.6	16.0	1.38	0.6	16.5	1.35	0.6	19.0
53.0	1.50	0.8	14.0	1.65	0.6	14.0	1.65	0.7	16.0

7. FINAL AMPLIFIERS

A total of four amplifier units were constructed as a demonstration of the capability of InP Gunn devices to provide wide-band, low-noise amplification. One unit was built for Ka-band (See Figure 7.1) and three units for the 40-60 GHz band (see Figure 7.2).

The Ka-band unit utilized the staggered gain configuration shown in Figure 7.3. The first two amplifier stages were tuned for gain response at the high end of the band and the third and fourth stages were tuned for gain responses at the low end of the band. The high frequency amplifier stages were separated from the low frequency amplifier stages by an interstage isolator. A photograph of the Ka-band amplifier unit with the cover removed is shown in Figure 7.4.

The gain response of each of the four stages is shown in Figure 7.5. Reduced height amplifier circuits were used in all four stages. InP cathode notch diodes from wafer EE130 were used in the low frequency amplifier stages and from wafer EE119 in the high frequency amplifier stages. These measurements were made using a reflectometer. The gain responses were adjusted to achieve the flattest possible gain response of the final amplifier. The gain response of each amplifier was intentionally adjusted to fall off near the band edge in order to minimize excessive gain ripple or spikes which resulted from poor circulator return loss in these regions. The gain response and noise figures of the final amplifier unit are shown in Figure 7.6. Gain compression data is given in Figures 7.7 and 7.8. At 30 GHz, power output was +6.1 dBm at the 1 dB gain compression point. At 35 GHz, power output was +4.8 dBm at the 1 dB gain compression point.

FIGURE 7.1 KA-BAND AMPLIFIER

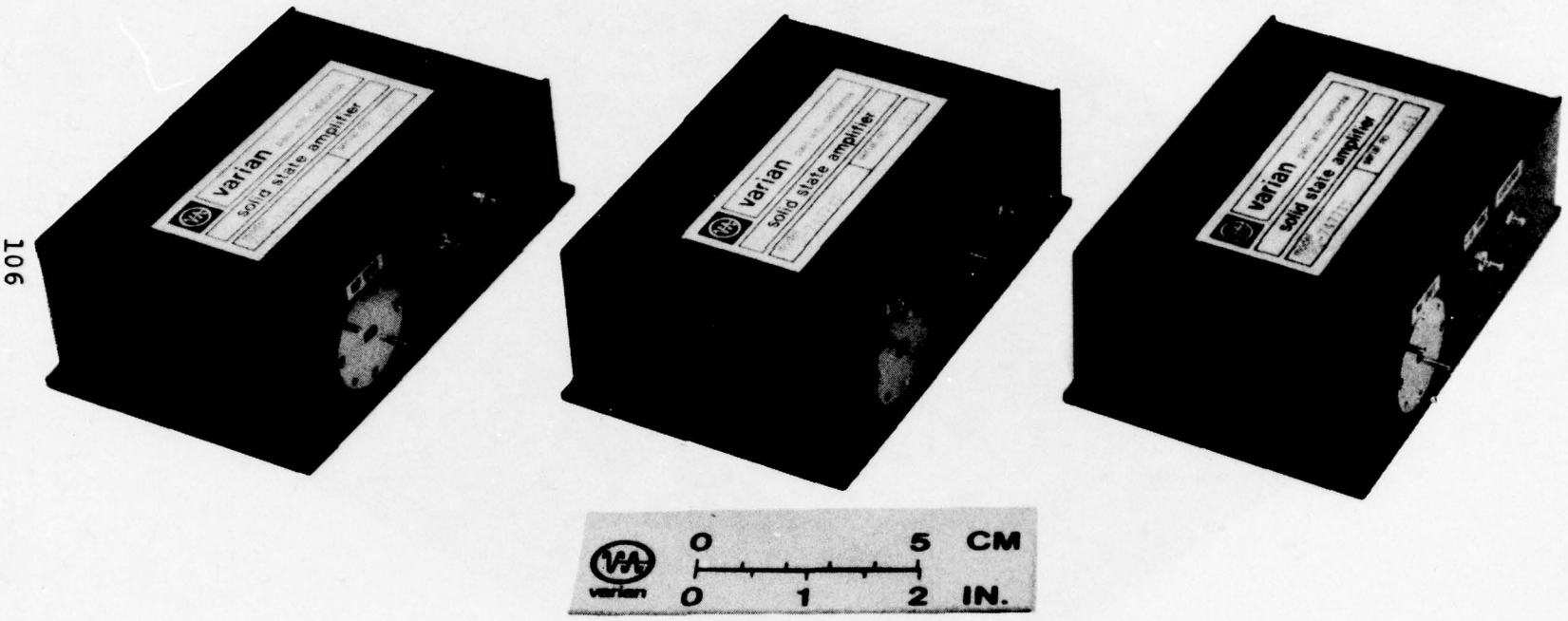


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FIGURE 7.2 THREE AMPLIFIERS FOR THE 40-60 GHz RANGE

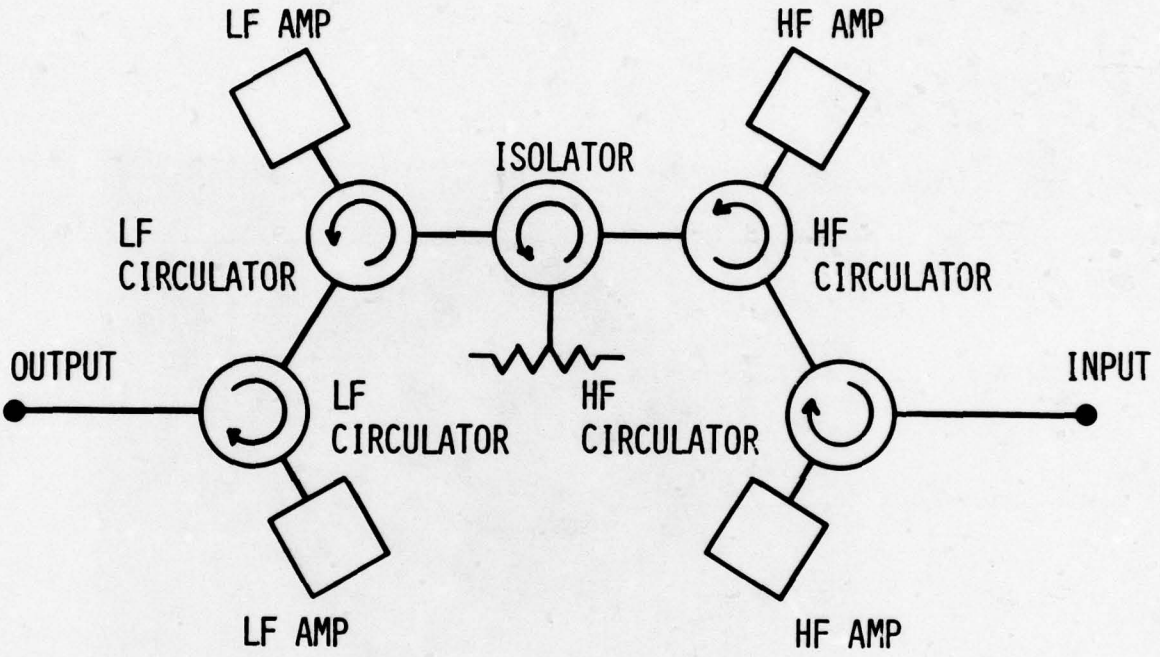

FIGURE 7.3 SCHEMATIC DRAWING OF K_A-BAND STAGGERED GAIN AMPLIFIER

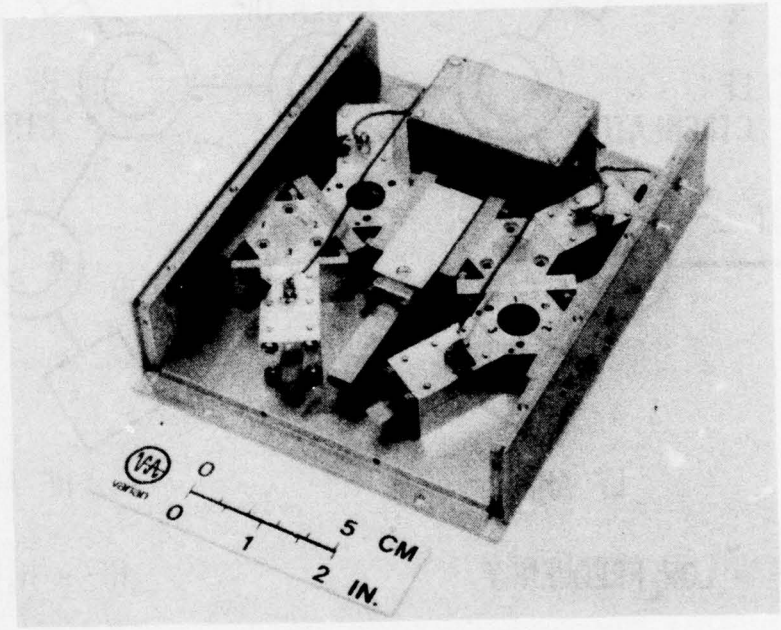

FIGURE 7.4 FINAL KA-BAND AMPLIFIER WITH COVER REMOVED

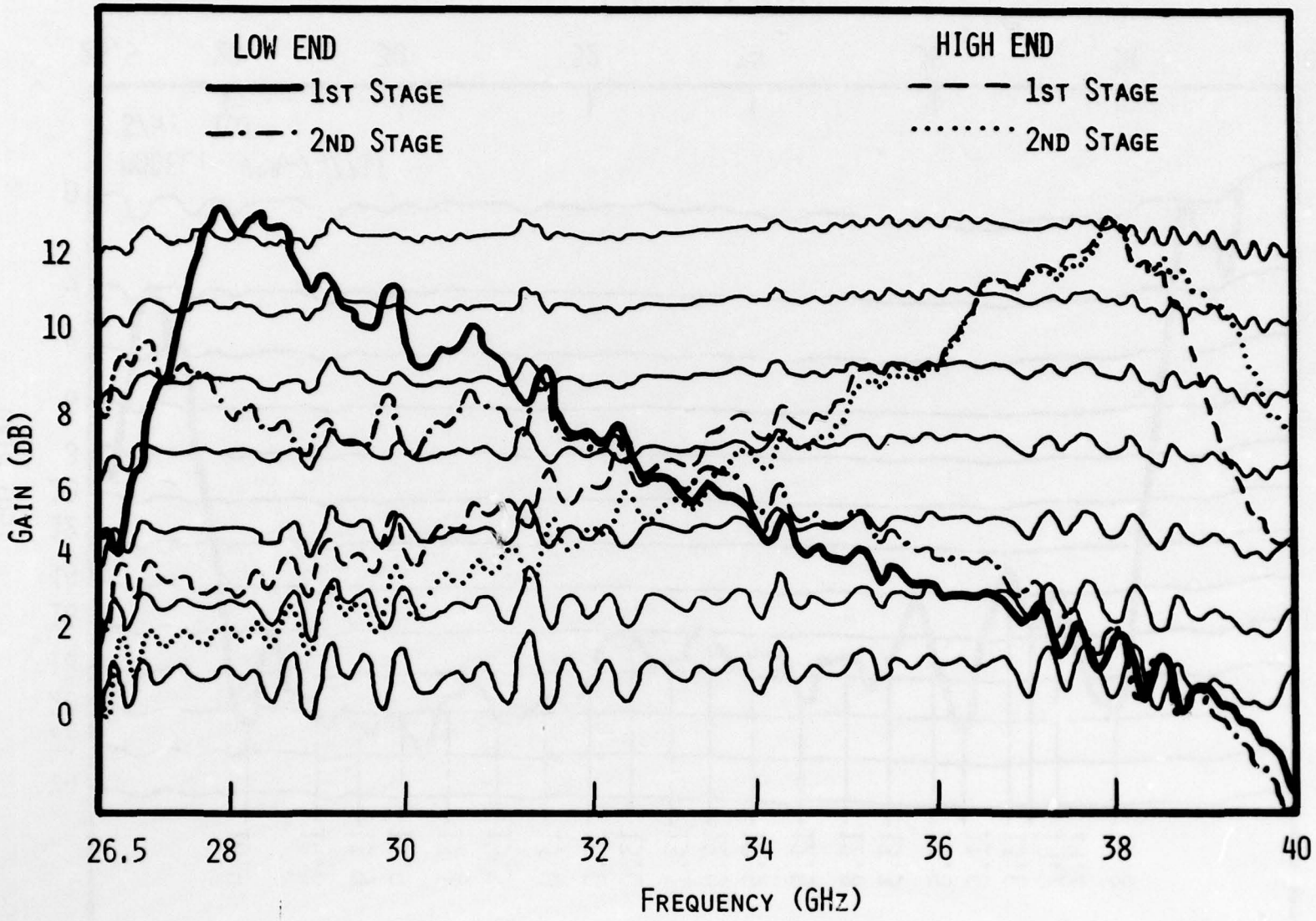

FIGURE 7.5 REFLECTOMETER GAIN RESPONSES OF THE FOUR INDIVIDUAL AMPLIFIERS USED IN STAGGERED GAIN FULL BAND AMPLIFIER

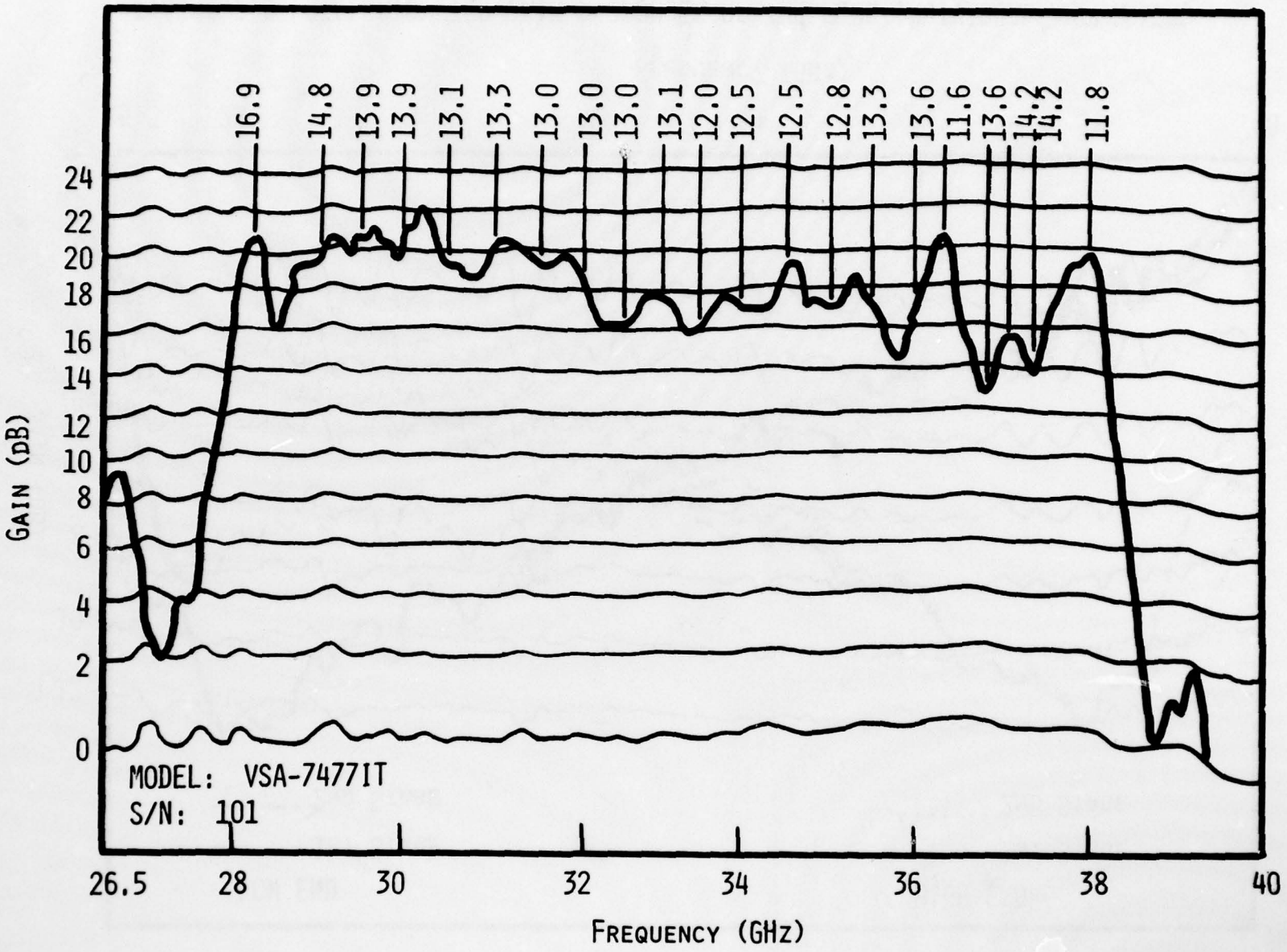

FIGURE 7.6 GAIN RESPONSE AND NOISE FIGURES OF FINAL Ka-BAND AMPLIFIER

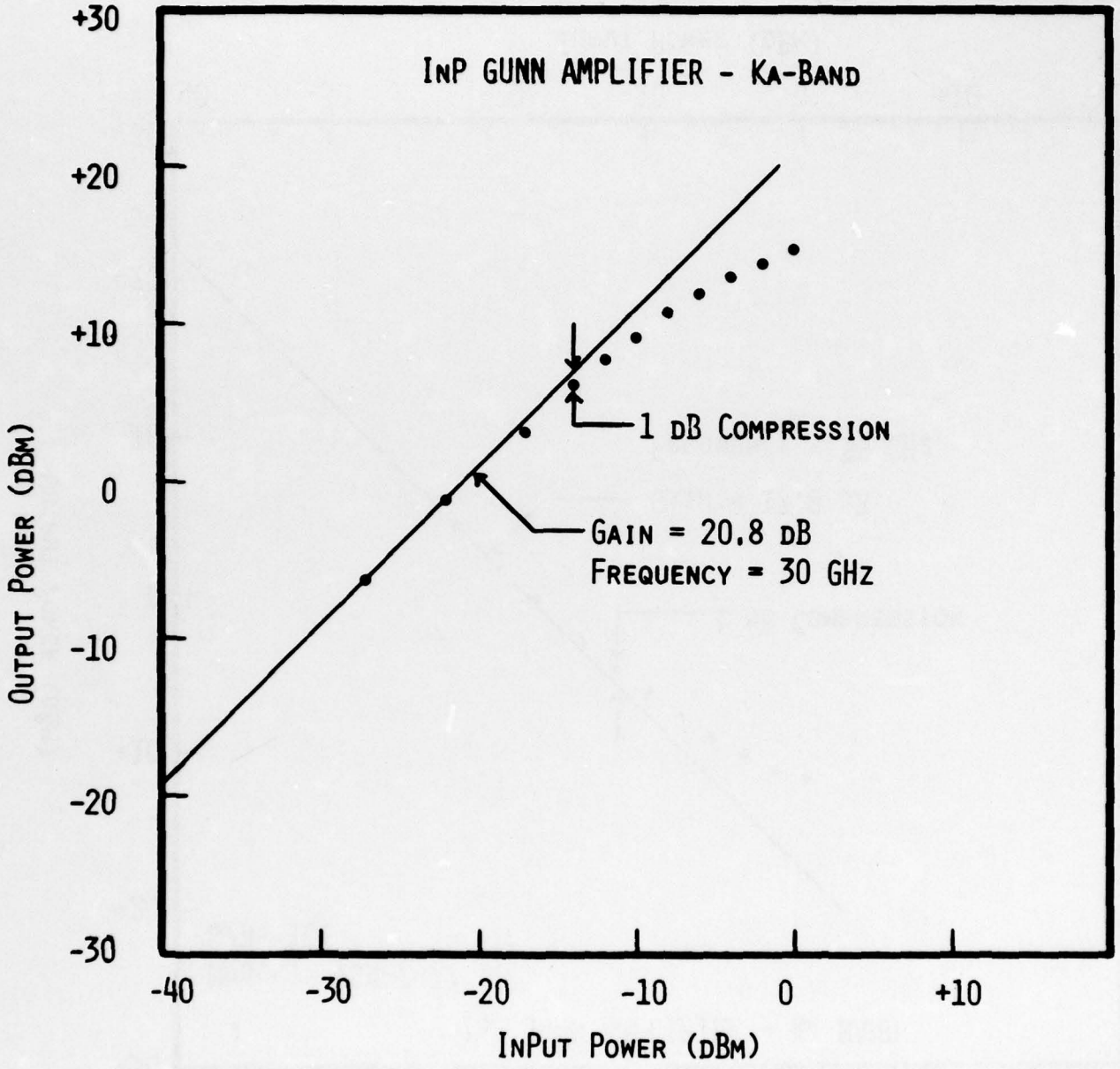

FIGURE 7.7 GAIN COMPRESSION DATA FOR Ka-BAND AMPLIFIER AT 30 GHz

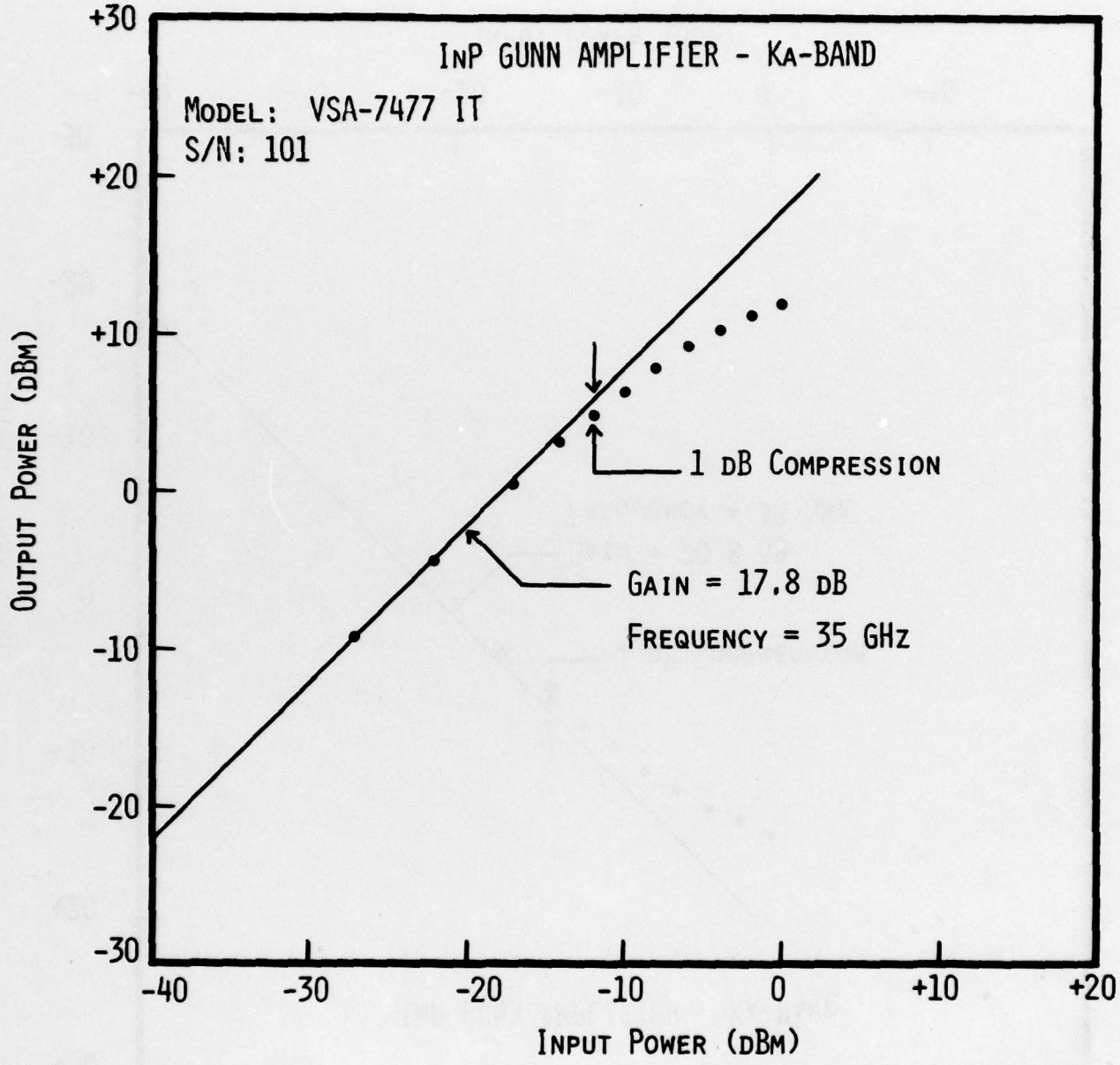

FIGURE 7.8 GAIN COMPRESSION DATA FOR Ka-BAND AMPLIFIER AT 35 GHz

Three units were constructed for the 40-60 GHz range. Nominal center frequencies of the units were 43.5, 50.0 and 56.5 GHz. A photo of one of the three units with the cover removed is shown in Figure 7.9. Each unit utilized a single stage reflection amplifier which consisted of a Y-junction circulator and a coaxial waveguide amplifier circuit. InP cathode notch diodes from wafer EE125 were used in all three circuits.

The gain responses, noise figures and gain compression data for each of the three amplifiers are given in Figures 7.10 through 7.15. Gain of 6 dB or greater was demonstrated throughout most of the 40-60 GHz band with noise figures between 10.0 dB and 11.0 dB. Power output at the 1 dB gain compression point was +12.0, +11.6 and +9.2 dBm for the 43.5, 50.0 and 56.5 GHz amplifiers, respectively.

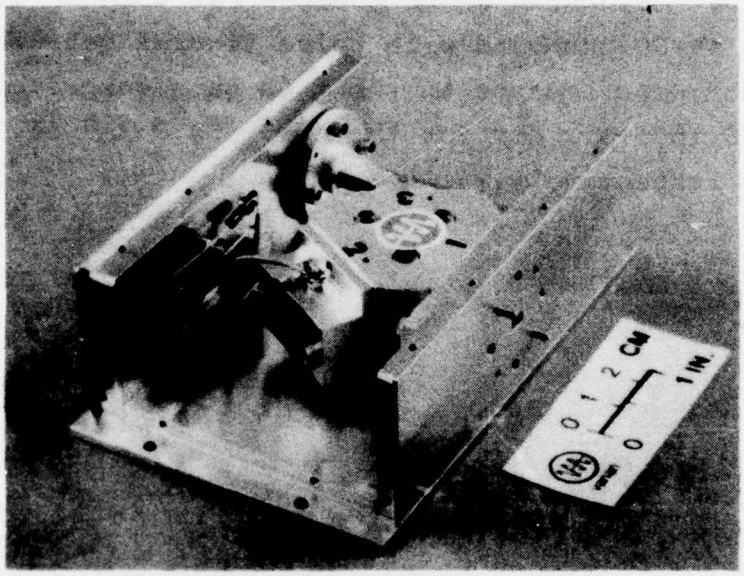

FIGURE 7.9 VIEW OF ONE OF THE AMPLIFIERS CONSTRUCTED FOR OPERATION IN THE 40-60 GHz RANGE

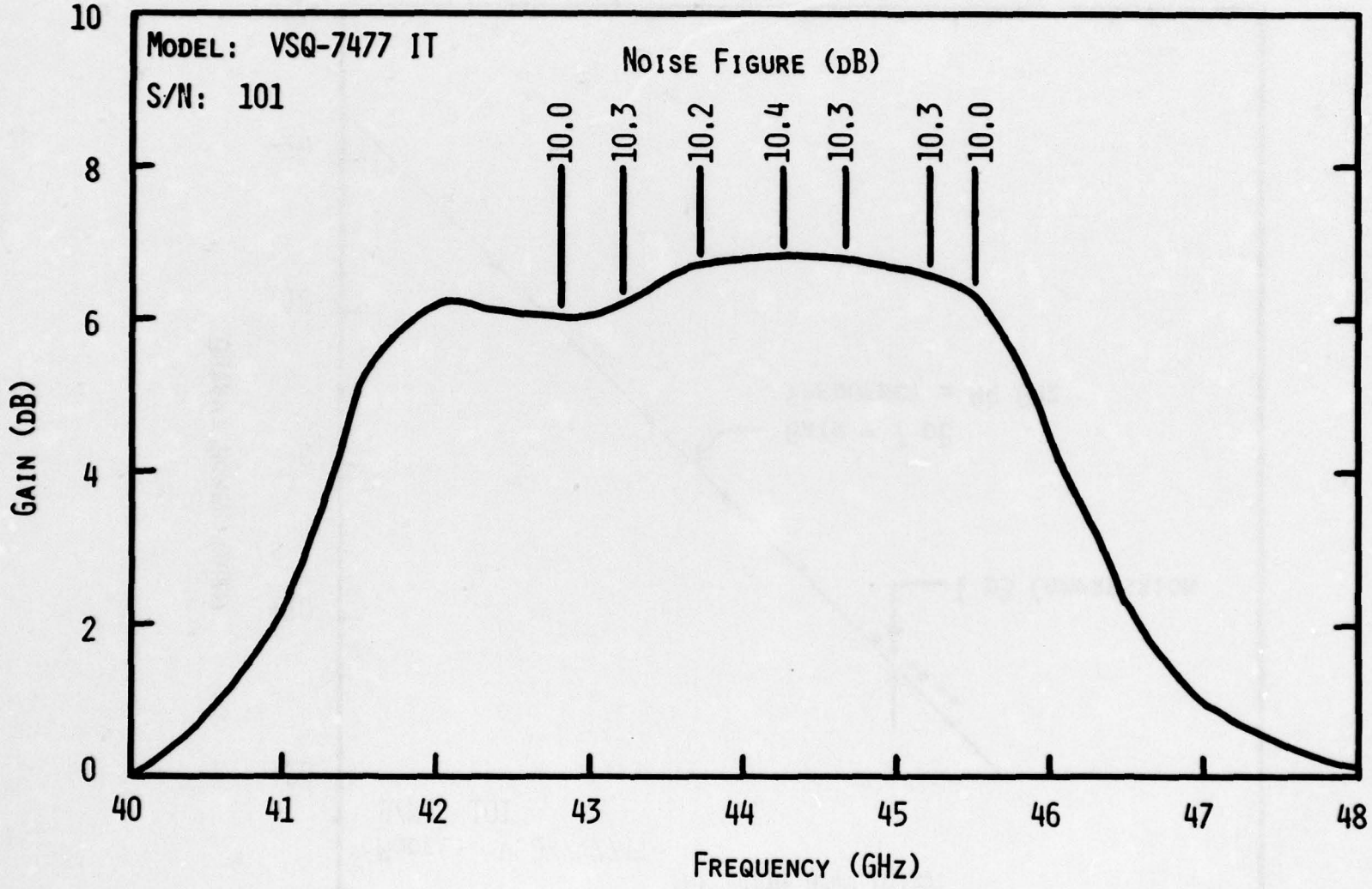

FIGURE 7.10. GAIN RESPONSE AND NOISE FIGURES OF 43.5 GHz AMPLIFIER

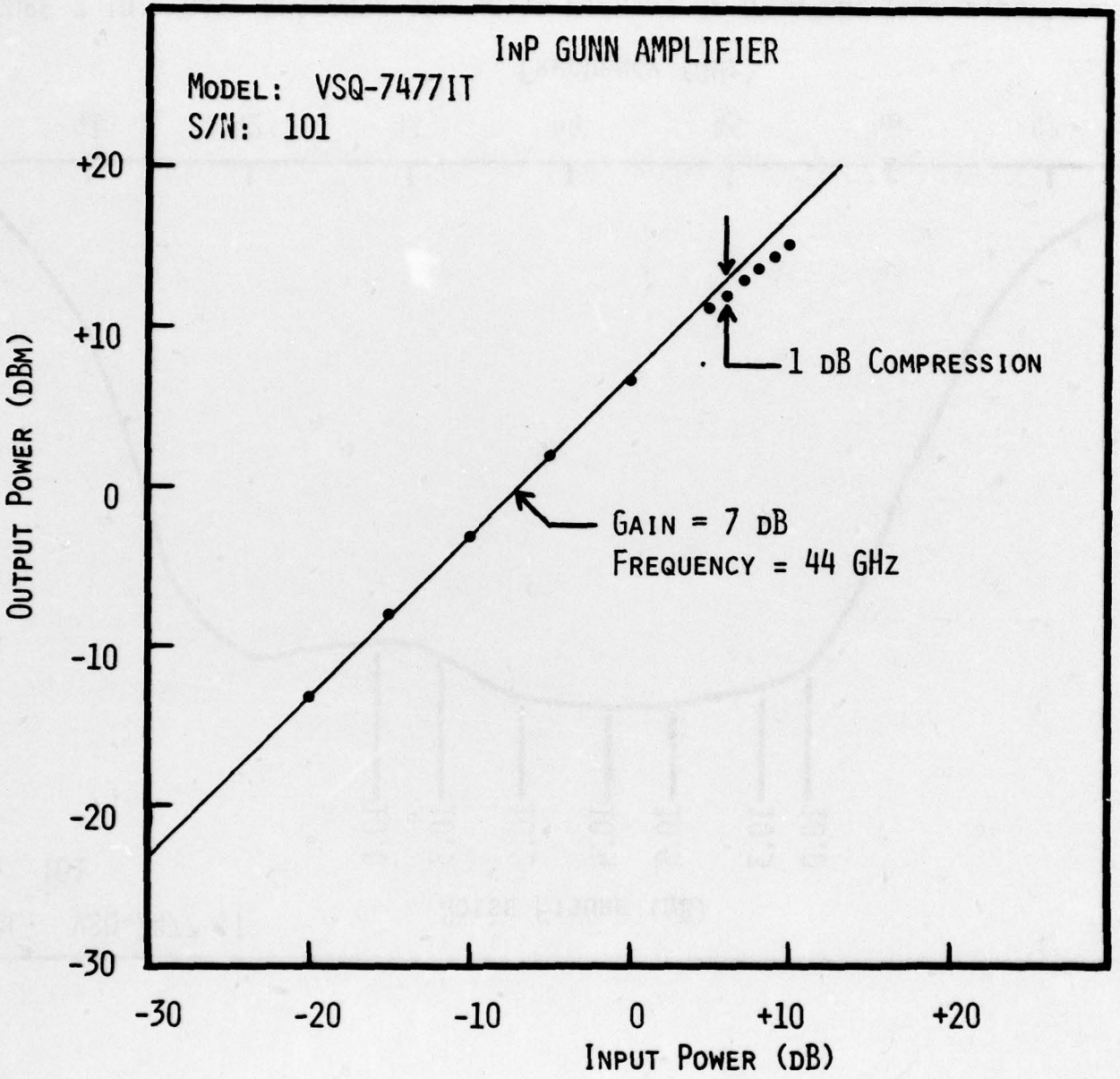

FIGURE 7.11. GAIN COMPRESSION DATA OF 43.5 GHz AMPLIFIER

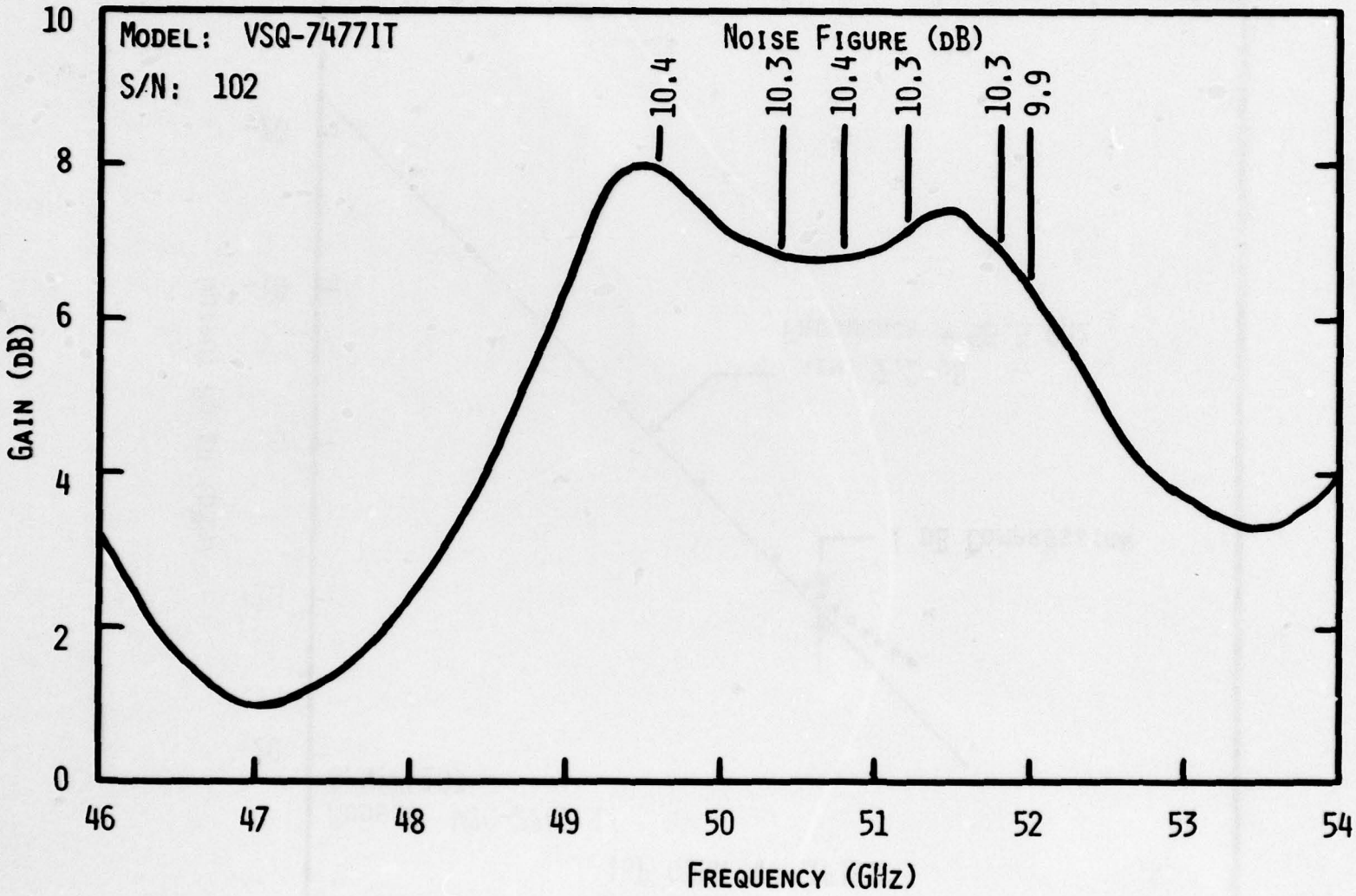

FIGURE 7.12. GAIN RESPONSE AND NOISE FIGURES OF 50.0 GHz AMPLIFIER

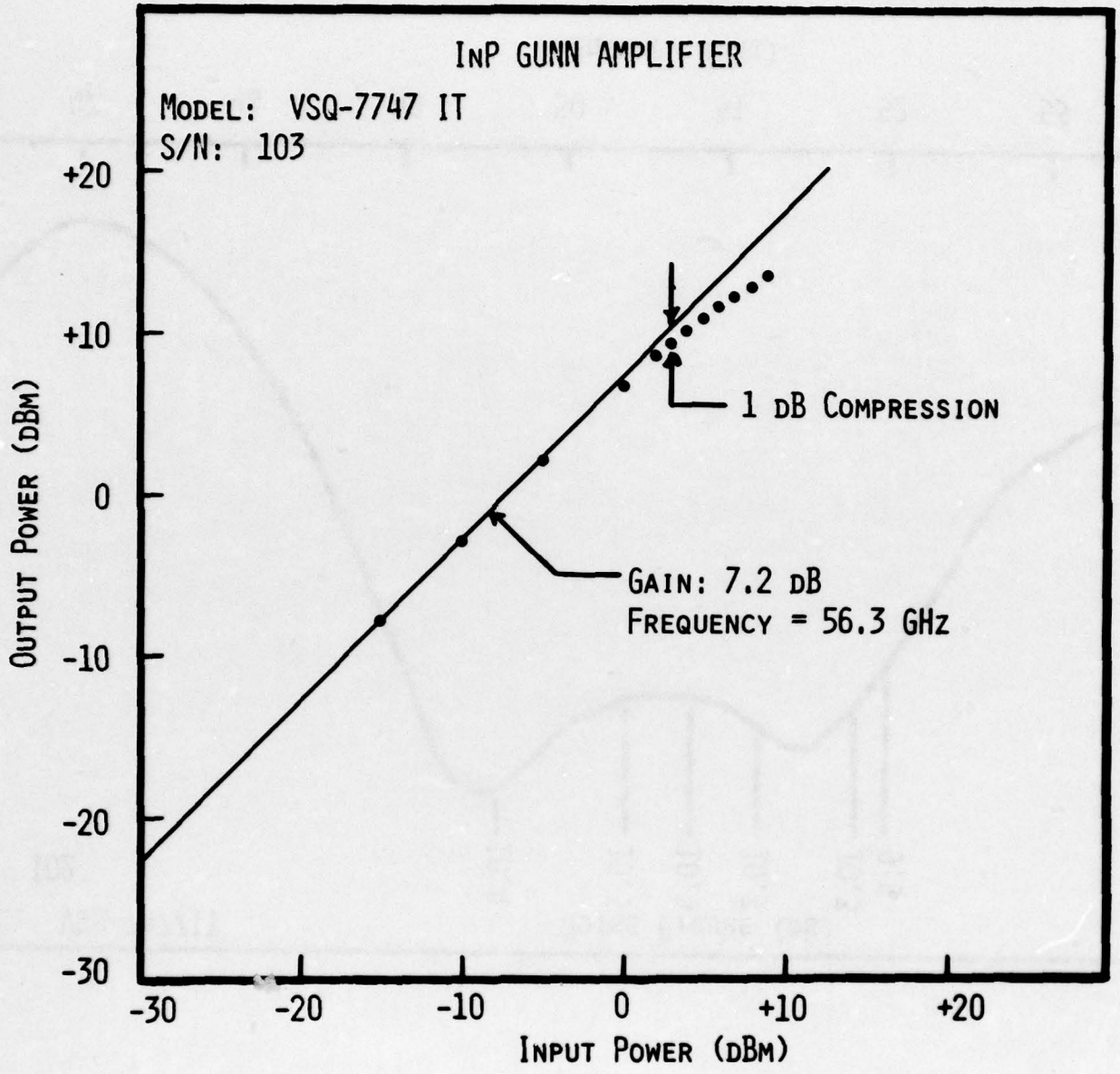

FIGURE 7.13. GAIN COMPRESSION DATA OF 56.5 GHz AMPLIFIER

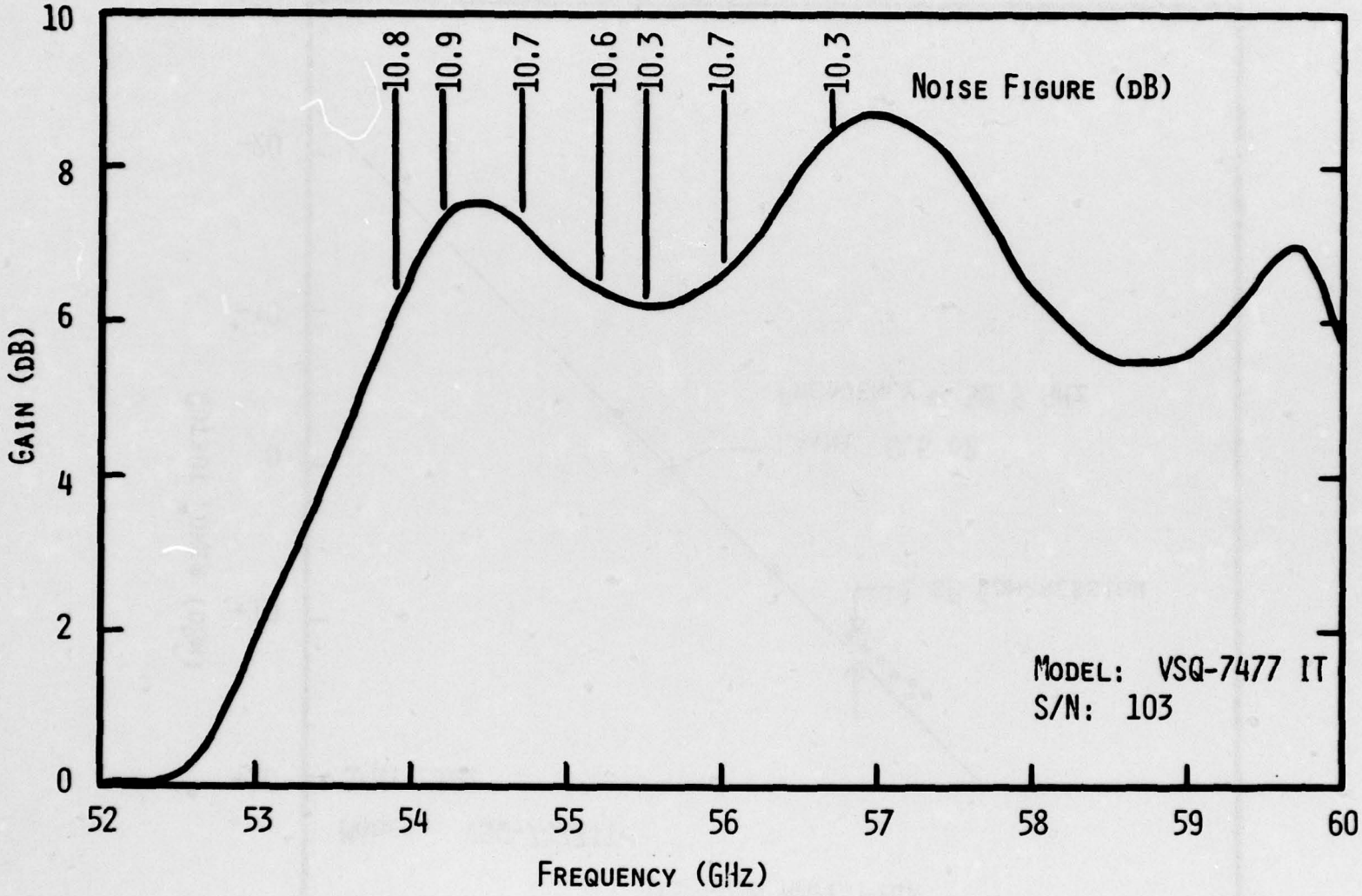

FIGURE 7.14. GAIN RESPONSE AND NOISE FIGURES OF 56.5 GHz AMPLIFIER

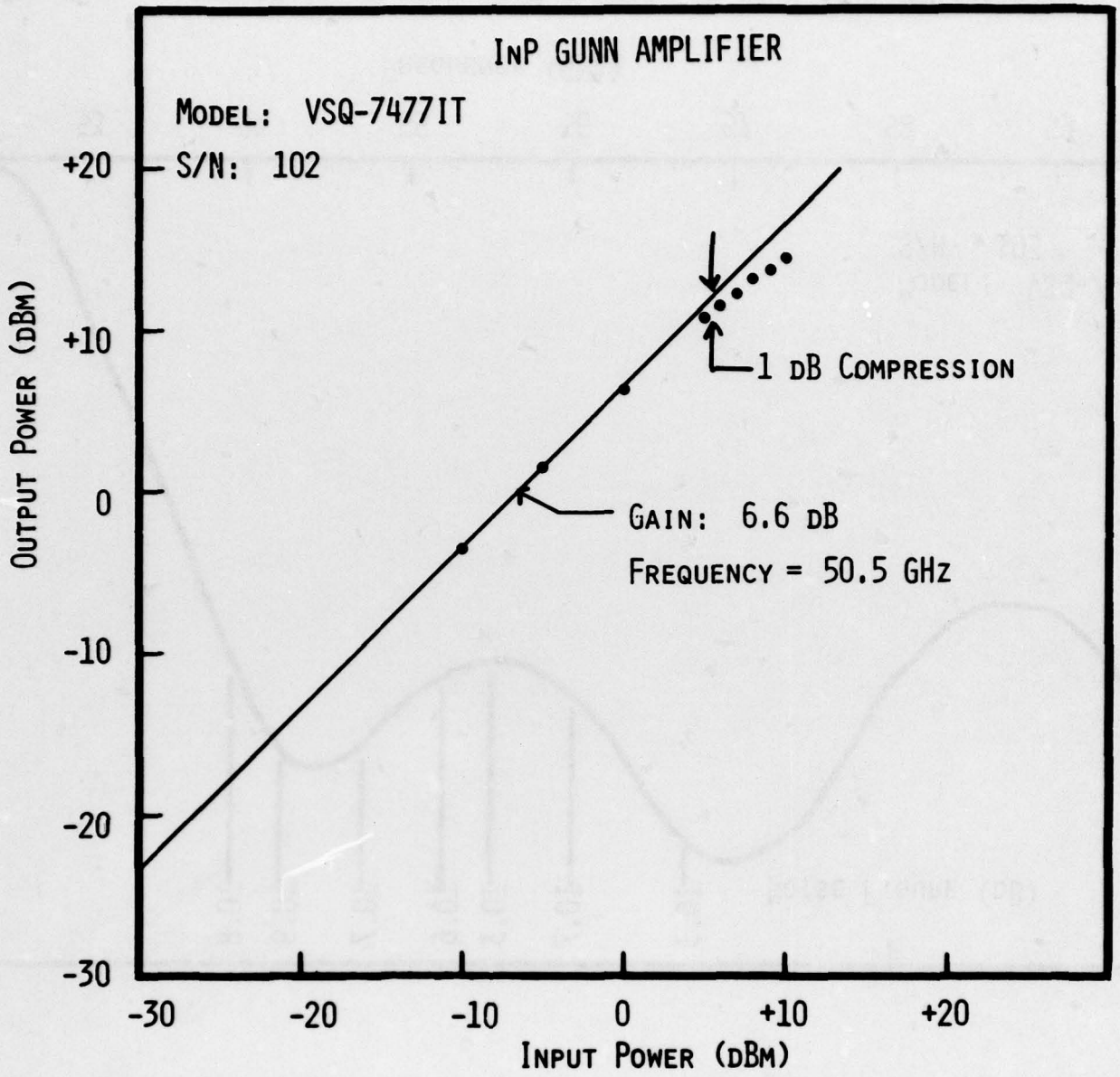

FIGURE 7.15. GAIN COMPRESSION DATA OF 50.0 GHz AMPLIFIER

8. CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE STUDY

The results obtained during this program demonstrate the superiority of InP over GaAs as a material for the fabrication of low noise, wideband millimeter wave Gunn amplifiers. Gains of 8 to 10 dB were achieved from InP Gunn diodes throughout the frequency range from 26.5 to 60 GHz. InP Gunn devices using a cathode notch structure have yielded noise measures as low as 7.7 dB in Ka-band. Very wide band results were demonstrated with an InP cathode notch device. Gain of 5 to 8 dB was obtained from a single device over an instantaneous bandwidth extending from 26.5 to 40 GHz. Typically, gains of 6 dB were obtained with noise figures of 8 to 9 dB.

There are several areas in which further development is required. Noise measures obtained to date with InP cathode notch devices are still 2 to 3 dB higher than has been predicted from theoretical models. This degradation in performance is attributed to the wide n^- notch which is required to produce uniform fields for low doped active layers. Considerable improvement should be obtained by using a p-notch structure. The performance of wideband amplifiers in Ka-band and the 40-60 GHz band is currently limited by the bandwidth of the circulators. Advanced development needs to be performed in the construction of wideband circulators specifically for Gunn amplifier applications. In addition, the development of microstrip amplifier circuits should be undertaken. The use of a hybrid coupled amplifier needs to be investigated as an alternative to the circulator coupled amplifier.

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